A Wideband Low Voltage Low Phase Noise 10-GHz SiGe Switchable VCO

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***Abstract* — This paper describes a fully integrated Silicon Germanium (SiGe) Voltage Controlled Oscillator (VCO) chip with 19% tuning range and low phase noise suitable for 10-Gb/s fiber optic transceivers and X-band applications. It consists of two switchable externally enabled VCO's. The total chip tuning range is 9.2-11.1GHz when the varactor control voltage varies from 0 to 3.0V and the measured phase noise is –87dBc/Hz at 100KHz offset from carrier. The typical current consumption is 8mA for the VCO core at 3.3V voltage supply. The chip is implemented in SiGe BiCMOS7 technology intended for high volume production.**

I. Introduction

The increasing demand of high-speed high complexity communication systems has led to a great interest in the integration of a large number of digital and RF functions on the same chip. Particularly in communication transceivers the VCO is one of the most critical building blocks. To ensure low power consumption and high spectrum efficiency, the VCO phase noise requirements are very stringent. The most important limitation for high spectral purity VCO's comes from the resonator quality factor Q. Integration of high quality factor passive networks is difficult because of losses due to silicon substrate and capacitive and inductive parasitics, whose effect is more important at high oscillation frequencies.
The main goal of this work is the achievement of a sustainable tradeoff between low phase noise and wide tuning range necessary to allow for process and temperature variations. However, the larger the bandwidth the higher the phase noise [1][2], as derived from Scherer extension of Leeson's formula (1):

$$L(f_m,K_{VCO}) = 10\cdot\log\left[\left(1+\left(\frac{f_o}{2f_m\cdot Q}\right)^2\right)\cdot\frac{FkT}{2P_s}\cdot\left(1+\frac{f_c}{f_m}\right)\right] \quad (1)$$

where $L(f_m,K_{VCO})$ is phase noise in dBc/Hz, f_o is oscillation frequency in Hz, f_m is frequency offset from the carrier in Hz, F is noise figure of the transistor amplifier, k is Boltzmann's constant, T is temperature in K, P_s is RF power of the oscillator in W, f_c is flicker noise corner frequency in Hz and Q is the tank quality factor.

Therefore it becomes crucial to choose a circuit topology that minimizes phase noise while mantaining large tuning bandwidth. This paper will describe the chosen architecture, the adopted design techniques and measured results.

II. Technology

The VCO is designed with a 0.25 μm SiGe HBT/CMOS technology from STMicroelectronics, suitable for system on-chip applications as it permits to combine RF and digital parts in a small area. The process has five metal layers with a thick (2.5 μm) upper metal for high Q inductor design, Metal-Insulator_Metal (MIM) capacitors, high resistive poly and P+/Nwell varactor diodes. The main features of the technology are shown in Table I for the minimum drawn geometry.

0.25μm SiGe HBT/CMOS technology	
F_t	70GHz
BV_{CEO}	2.6V
F_{max}	90GHz
h_{fe}	100
C_{ie}	2.7fF
C_{ic}	2.67fF
C_{is}	5.24fF

TABLE I

MAIN TECHNOLOGY PARAMETERS FOR THE MINIMUM DRAWN GEOMETRY

A. Tank Inductors modeling

VCO tank high-Q inductors have been drawn with inductance values computed by means of formulas reported in [3] that take into account the mutual inductance of close conductors and have been modified to apply to octagonal-shaped inductors. The calculated inductance has been checked against a three dimensional inductance extraction program while parasitic capacitance has been extracted by Cadence environment tools. A patterned ground shield under the inductors has been drawn to reduce Eddy currents and current flowing through substrate resistance [4]: practically, only losses due to metal traces are significant.
To correctly model tank inductors, a quasi-distributed model instead of a simple T or Π model has been built: a T-like model underestimates capacitive parasitics (increasing tuning bandwidth) while a Π-like model

overestimates them (reducing tuning bandwidth). The higher the number of stages of the quasi-distribute model, the better the accuracy. Practically, a simple two-stage hybrid model ensures a good accuracy in predicting tuning bandwidth.

III. VCO CHIP TOPOLOGY

The chip consists of two switchable VCO's, each one with its own buffer, followed by a selection circuit to provide a good isolation between the two paths (Fig. 1). VCO's, buffers and the selection circuit are externally enabled using the ENVCO pin. VCO selector consists of two differential pairs whose reference current is switched properly. For operating and measurement opportunities the output is either differential for 100-ohm load or single-ended for 50-ohm load. The 50-Ohm matching in the output buffer is obtained by carefully dimensioning resistive loads and transistor size of the differential pair, taking into account bond-pad parasitic capacitance and bond-wire inductance.

In VCO cores and related buffers separate bias supply lines have been used to reject noise and reduce crosstalk. For the same purpose, tank inductors of the two VCO's have been positioned on one side of the chip, isolated from the rest of the circuitry.

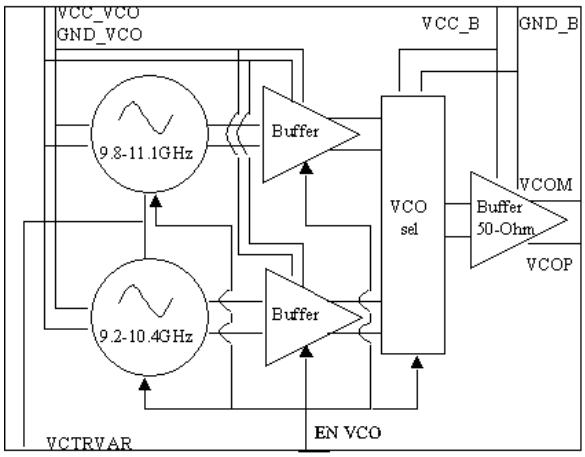

Fig. 1 Switchable VCO IC block scheme. VCO cores (and the following buffers) have separate supply lines to avoid cross-talk and reject noise.

A. VCO's core

A simplified schematic of VCO cores is depicted in Fig. 2. The active part of the oscillator is composed of a cross-coupled differential pair with capacitive coupling. A direct DC cross-coupling between transistors of the differential pair would enlarge tuning bandwidth (decreased parasitic capacitance on tank nodes) but would, at the same time, degrade noise performance (differential pair works in saturation region, V_{CB} = 0V, V_{CE} = V_{BE} ≈ 0.9V). Large transistors with low base, collector and emitter resistances are used in order to minimize thermal noise. The optimum simulated bias current that minimizes phase noise introduced by BJT's (as described in [5]) is about 10mA (Fig. 3).

To improve Common Mode Rejection Ratio (CMRR) and filtering phase noise (as proved in [6]), a patterned inductor has been inserted in the tail current source (Fig. **2**).

The main guidelines followed in VCO design to achieve optimum trade-off between phase noise and tuning range are listed in the following sections.

The first simple design rule is to separate the nodes from which one withdraws the VCO signal from the nodes across the tank. If the signal is withdrawn from the bases of the transistor pair and not from the collectors, the quality factor of tank will not be degraded and the circuit will be less sensitive to load pulling.

The second key point is to carefully evaluate parasitic capacitances and inductances from interconnections that can shift the oscillation frequency and degrade phase noise. Usually, extraction programs provide only capacitive and resistive parasitics and neglect inductive parasitics that have to be calculated using analytical formulas or EM simulators.

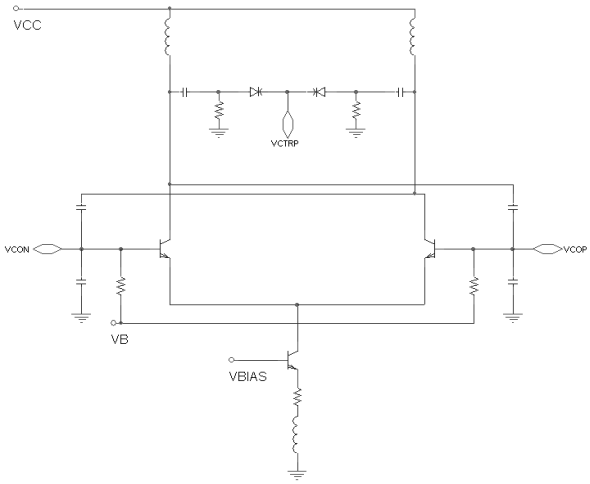

Fig. 2 VCO's core simplified schematic. The differential pair is cross-coupled through capacitors to produce the negative resistance necessary to compensate for the loss in the resonator.

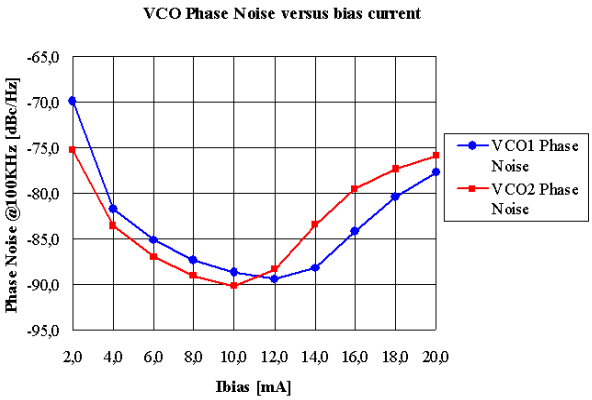

Fig. 3 VCO's core phase noise versus bias current. For both VCO's, a minimum in phase noise is obtained for bias current between 8-12 mA.

In the third place, it is necessary to closely choose the varactor area: the larger the varactor the wider the tuning

bandwidth but the higher the phase noise introduced[6]. It would be very convenient to provide a path to ground low frequency noise: this can be done by biasing the varactor diode through an inductor and ac coupling the varactor itself to the tank nodes by means of series capacitors.

Obviously, these capacitors have to be large not to limit varactor tuning range. The associated parasitics (both resistive and capacitive to substrate) have to be taken into account. As a drawback, the area occupied by each VCO would double, mainly due to these new bias inductors: to avoid this, resistors have been used instead of inductors to bias the varactors, providing a loss of about 1.5dB in simulated phase noise.

IV. RESULTS

Naked chips have been wire bonded on Ar1000 substrate (ε_r=9.8) as showed in Fig. 4. External components such as resistors and capacitors have been placed on the boards to clean DC bias lines from the noise injected by power supplies and batteries have been used for the varactor tuning voltage.

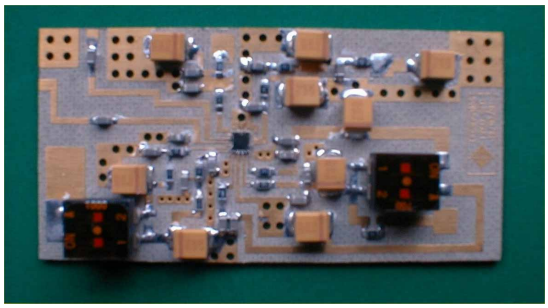

Fig. 4. Wire bonded naked chip. The substrate used to realize the board is Arlon1000 (ε_r=9.8). To enable VCO1 or VCO2 the switches visible on the board are used.

Fig. 5 and Fig. 6 show the comparison of simulated and measured VCO chip results operating in free running mode. The measurements have been performed in single ended mode, with a 50Ohm termination on the other differential output. The good agreement between measured and simulated oscillation frequency and phase noise validates the adopted design metodology. The main features of the VCO chip are 1.9GHz tuning bandwidth (19%) and –87dBc/Hz phase noise at 100KHz offset. The tuning range remains almost constants over bias voltage and temperature variations. Measured results are summarized in TABLE II.

To benchmark VCO's in different frequency bands and with different power consumptions, a Figure of Merit (FOM) has been calculated for each VCO as in (2):

$$FOM = £meas(f_{offset}) - 20 * \log(f_{osc} / f_{offset}) + 10\log(Pdiss / 1mW) \quad (2)$$

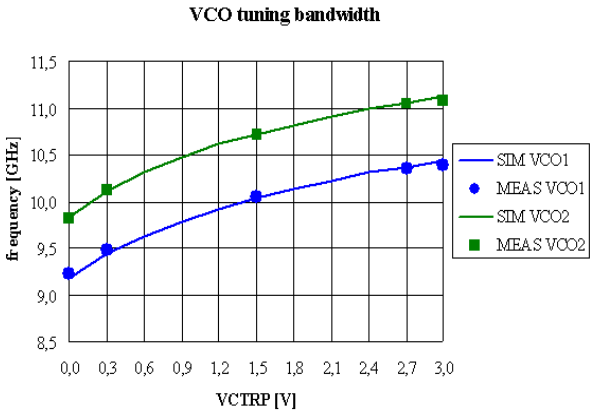

Fig. 5. Simulated and measured VCO's tuning bandwidth at 100KHz offset from carrier (9.2-10.4GHz for VCO1 and 9.8-11.1GHz for VCO2 when VCTRP varies from 0V to 3.0V).

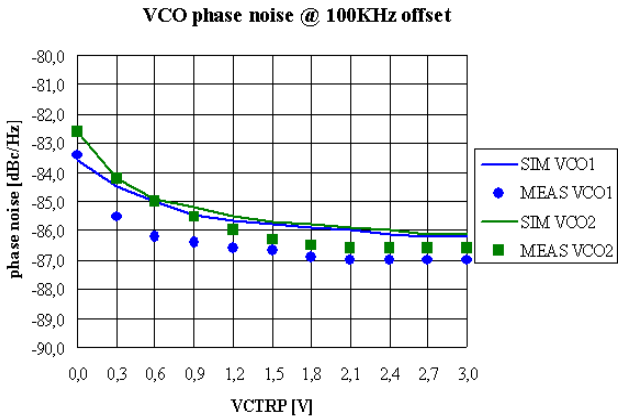

Fig. 6. Simulated and measured VCO's phase noise at 100KHz offset from carrier when VCTRP varies from 0V to 3.0V.

where £meas is measured phase noise at a frequency offset f_{offset} from the center frequency f_{osc} and *Pdiss* is the VCO power dissipation in milliwatts.

Using this definition, a FOM of about –174dBc/Hz is obtained for both VCO's. This is one of the best FOM reported in literature [6][7], particularly taking into account the large tuning bandwidth obtained (13% for each VCO and 19% for VCO chip).

Features of 1.9GHz tuning range VCO	
Tunability Range VCO1 Tunability Range VCO2	9.2-10.4GHz 9.8-11.1GHz
Phase Noise @10.15GHz	-87dBc/Hz @ 100KHz
Voltage Bias Supply	2.7-3.6V
Total Iass	47mA
VCO core Iass	8mA
FOM VCO1 e VCO2	-174dBc/Hz

TABLE II

MAIN FEATURES OF VCO CHIP

V. CONCLUSION

A fully integrated SiGe 10GHz VCO has been described, which performs low phase noise (-87dBc/Hz @100KHz) and very wide tuning bandwidth (19%) at low voltage bias supply. A very good trade-off among phase noise, tunability and power consumption has been achieved using a SiGe commercial technology and the developed chip covers the desired working frequency against process spread, temperature and supplies variations, thus decreasing costs for high volume production.

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