Device-level Intermodulation Distortion Control on III-V FET's

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Abstract — **Highly linear and efficient amplification is currently a hot topic in the RF/microwave community. Special interest is being paid to those low cost and simple solutions able to be implemented in current and future mobile terminals. Device-level intermodulation distortion (IMD) control represents a key element in this research effort, since it allows both the optimization of the transistor linearity performance and the development of novel device-based linearization techniques. In this paper, the main IMD characteristics of III-V FET's are remarked, either on small- or large-signal regime, to show the potentialities of different operating conditions for the design of highly linear amplifiers. Some promising linearization topologies, based on these characteristics, are then considered. Finally, the spatial power combining feature of certain radiating structures is incorporated in such topologies, resulting in highly integrated solutions.**

I. Introduction

Modern wireless systems relay on the use of digital modulation formats and multiple carriers. The resulting signal, to be transmitted and received, has usually a complex and strongly time-varying envelope, reason why stringent linearity requirements are imposed to the RF processing blocks. The battery powered nature of the mobile terminals, mostly used in these systems, also places a premium on the efficiency performance, particularly for the power stages. In this context, the tremendous interest in the design community for solving the trade-off between linearity and efficiency, can be perfectly understood. Novel linearity enhancement techniques have appeared, and those based on the active device performance are receiving a lot of attention [1-4].

As mildly nonlinear devices, an accurate control of MESFET/HEMT intermodulation distortion (IMD) requires a dedicated model extraction able of reproducing not only the nonlinear *I/V* and *C/V* characteristics but also their higher order derivatives.

In this paper, the main IMD characteristics of typical III-V FET's, arising from particular nonlinear characterization procedures, are highlighted. The potentialities of different operating conditions, either on small- or large-signal regime, for improving linearity are considered. Those linearization topologies, developed over the device characteristics, are also discussed. Finally, the spatial power combining feature of certain radiating structures is incorporated in such topologies, resulting in highly integrated solutions.

II. Higher Order Derivative Role

A. Small-signal regime

The role of nonlinearity derivatives on device small-signal nonlinear performance has been described some years ago [5-6]. The drain current source stands as the main IMD contributor, reason why it deserves most of the attention. A generally accepted terminology for the Taylor-series expansion of this nonlinearity in terms of the gate-to-source and drain-to-source voltages is presented in Eq. 1

$$\begin{aligned} Ids(Vgs,Vds) &= I_{DS}(V_{GS},V_{DS}) + Gm1\cdot vgs + Gds\cdot vds + \\ &+ Gm2\cdot vgs^2 + Gmd\cdot vgs\cdot vds + Gd2\cdot vds^2 + Gm3\cdot vgs^3 + \\ &+ Gm2d\cdot vgs^2\cdot vds + Gmd2\cdot vgs\cdot vds^2 + Gd3\cdot vds^3 + ... \end{aligned} \tag{1}$$

A simplified analysis of the equivalent circuit rejecting the influence of the reactive elements and applying Volterra-series approach, takes us to an expression of the in-band third order IMD current dependent on *G3* parameter,

$$\begin{aligned} G3 &= {}^{kgs^3}\!/\!_{\Delta}\cdot\left(Gm3 + kv\cdot Gm2d + kv^2\cdot Gmd2 + kv^3\cdot Gd3\right) + \\ &+ {}^{kgs}\!/\!_{\Delta}\cdot\left(2\cdot krg\cdot Gm2 + (krd + kv\cdot krg)\cdot Gmd + 2\cdot kv\cdot krd\cdot Gd2\right) \end{aligned} \tag{2}$$

where

$$\Delta = 1 + Gm1\cdot Rs + Gds\cdot(Rs + Rd + RL) \tag{3}$$

The *kgs* coefficient relates de amplitude of the gate-to-source first order control voltage with the generator amplitude, while *kv* is the intrinsic voltage gain. *Krg* and *krd* represent the contribution of the nonlinear current source to the corresponding voltage when analyzing the second order circuit.

Except for those points with optimum linearity (minimum contribution of the third order terms), the influence of the second order coefficients has been shown to be of minor significance [6]. An equivalent *Gm3*, a sort of third order parameter as the extracted in the simplified approach [5], could include all the third order term contributions:

$$Gm3eq = Gm3 + kv\cdot Gm2d + kv^2\cdot Gmd2 + kv^3\cdot Gd3 \tag{4}$$

1) Bias control in normal load conditions

If we consider as "normal" those R_L values not determining a high voltage gain, $kv < 10$, we could approximately neglect the contribution to $Gm3eq$ of the third order cross and output terms. In this situation, $Gm3 \cong \partial^3 Ids/\partial Vgs^3$ would be responsible for the device IMD performance. In Fig. 1 we show the $Gm3$ evolution versus V_{GS} and V_{DS} bias voltages for a typical HEMT, the NE3210s01 from NEC.

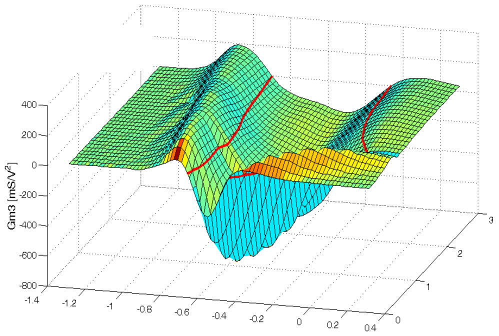

Fig. 1. $Gm3(V_{GS}, V_{DS})$ evolution for a typical HEMT

We can appreciate the existence of two null regions, one corresponding to the pinch-off transition and other appearing for high V_{GS} values. The first null seems not to be very useful for small-signal applications as the associated gain is quite low, however, the second one appears in the high transconductance region and is responsible for the small-signal linearity sweet-spot reported in class A amplifiers (mainly evident in those based on MESFETs).

Two regions are easily differentiated around the Vp null, where the $Gm3$ value could be controlled in an important range and with both signs, allowing the conception of simple device-level linearization topologies.

2) Load control

Controlling the load value, it could be possible to modify the V_{GS} values where $Gm3eq$ is null, due to a higher contribution of the cross and output terms. That situation is responsible for the existence of one or two zones of optimum linearity in a MESFET small-signal amplifier under load-pull conditions. It should also be considered when trying to take advantage of the $Gm3eq$ performance around pinch-off in the device-level linearization techniques. In Fig. 2, as a way of illustration, we show the $Gm3eq$ evolution in terms of V_{GS} and R_L for the same HEMT at $V_{DS}=3V$.

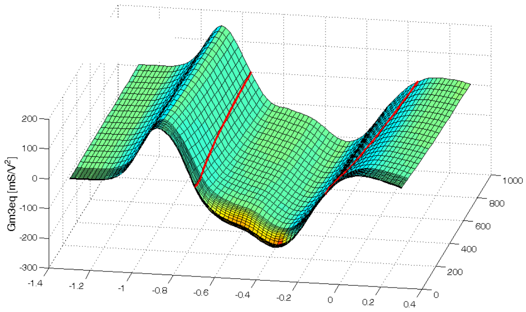

Fig. 2. $Gm3eq(V_{GS}, R_L)$ evolution for the NE3210s01

B. Large-signal regime

Linearity sweep spots do not only exist in small-signal regime but also in large-signal operation. The origin of this particular behavior has been recently explained [7], associated to the difference in phase between the small- and large-signal in-band IMD currents. In the conditions of operation near saturation, it has no sense describing the device performance through the bias point derivatives, but an acceptable approach over the useful range of input power may be obtained when substituting these parameters by the mean value of the time-varying Taylor-series coefficients [8].

1) Bias control in normal load conditions

In Fig. 3, we show the evolution of $\overline{Gm3eq(t)}$ nulls for the above device versus V_{GS} and Pin at $V_{DS}=3V$ and 50Ω load condition. It is possible to distinguish a region of input power variation where the zeros stay at a fixed V_{GS} value (small-signal regime), and a higher input region where these nulls experiment a significant input power dependence (large-signal operation). The "useless" $\overline{Gm3eq(t)}$ zero appearing in pinch-off for low input power levels seems to become attractive for higher levels as in this kind of operation is a common practice to change class A gain for class AB or class B efficiency. A dual bias control in this conditions might even assure these points to appear with the desired gain for a significant Pin range.

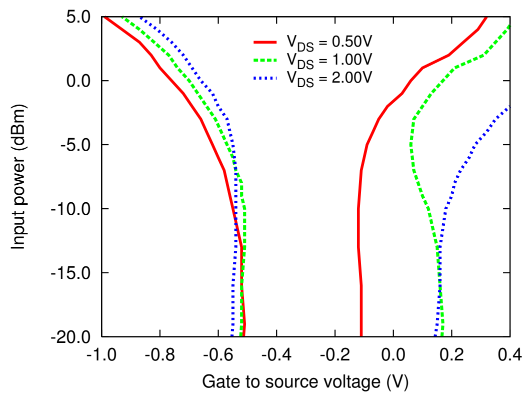

Fig. 3. $\overline{Gm3eq}(V_{GS},Pin)$ null evolution for three V_{DS} values.

2) Load control

A recent paper has detailed the influence of R_L in large signal regime [9]. The load contribution through the mean values of the time-varying cross and output terms may even produce the large-signal nulls to disappear. This influence could be critical if we try to use the change of sign appearing in $\overline{Gm3eq(t)}$ around the plotted large-signal nulls.

III. Device-level linearization techniques

Different techniques could be implemented based on the characteristics of the device performance either on small- or large-signal operation [1- 4]. Some of them are inspired on the classic system-level techniques while other are quite particular of the transistor characteristics. In both cases, we could talk of a main device whose IMD wants to be minimized and of an auxiliary transistor able of providing the distortion components with the proper phase to assure the cancellation. The techniques could be grouped, for instance, according to the order of the derivative used to produce the IMD cancellation in the main device:

- Second order based techniques
- Third order based techniques

In the first group, those techniques using the feedback or feedforward of the envelope or/and second band distortion components may be included [1, 2]. As previous sections have been focused on the third order coefficient role, our emphasis here will be put in some relevant techniques included in the second group.

A. *Small-signal regime*

1) Predistortion

A typical small-signal device-level predistortion topology has been presented in [3]. Adjusting the voltage applied to the auxiliary device gate terminal, just around the pinch-off value, a bi-phase amplitude control of its in-band IMD current could be produced with an associated low gain. In this way, it is possible to cancel the distortion of the main device without affecting its gain.

2) Derivative-superposition

This technique was proposed in [4], and has derived in an important set of promising variants during the last years. A gate-voltage control under pinch-off of an auxiliary device with the proper size may produce a *Gm3* contribution contrary to the one of the main transistor, canceling the in-band IMD current at drain side.

B. *Large-signal regime*

There seems not to be limitation to extend previous techniques to large-signal operation. The main obstacle has been due to the fact that the origin of the device particular performance in such regime has not been clear until the appearance of very recent works [7, 9].

However, large-signal operation uses to impose requirements hard to be satisfied through the small-signal linearization conception. As a way of illustration, the use of auxiliary devices with no gain contribution deteriorates the efficiency figures of merit, something generally unacceptable with the levels handled in power amplifiers.

1) Predistortion

Different efforts have been dedicated to use a preamplifying stage as predistorter. At device level, we could think on adjusting the gate voltage around the point of null $\overline{Gm3eq(t)}$ for the input power level to be handled, giving rise to an in-band IMD current with controllable amplitude and with two opposite phase values. When doing this, the gain is slightly modified, also affecting the IMD performance of the main device. Nevertheless, this could be corrected if conveniently adjusting V_{DS} in the main device.

An optimum linearity could be then obtained when the auxiliary device IMD contribution, amplified by the main transistor (Eq. 5a), were able of canceling the main device IMD component (Eq. 5b).

$$\overline{Gm3_{eq}(t)}_A \approx - \overline{Gm3_{eq}(t)}_{aux} . Zin_{main} . \overline{Gm1_{eq}(t)}_{main} \quad (5a)$$

$$\overline{Gm3_{eq}(t)}_B \approx - \overline{Gm1_{eq}(t)}^3_{aux} . Zin^3_{main} . \overline{Gm3_{eq}(t)}_{main} \quad (5b)$$

where $Gm1eq = Gm1+kv.Gds$, and Zin_{main} is the input impedance of the main FET.

A cascade connection of two NE3210s01 devices was implemented to consider the possibility of producing a large-signal sweet spot for the connection. In Fig. 4, both *Pout* vs. *Pin* IMD contributions are plotted to show the point resulting in the combined sweet-spot (*).

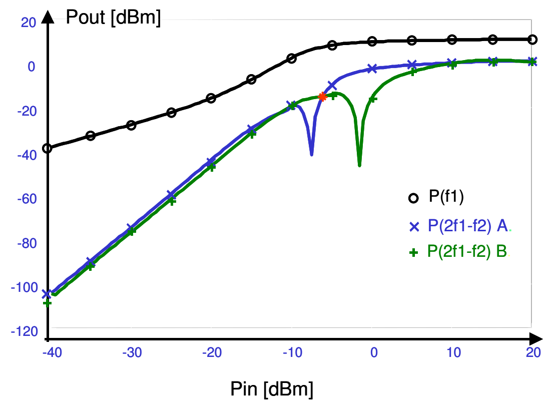

Fig. 4. Pout vs. Pin characteristic for each contribution to the cascade connection IMD. A and B represent the contributions in Eq. 5a and Eq. 5b respectively.

2) Derivative superposition

A first large-signal extension of the derivate superposition technique was recently proposed by the authors of the small-signal technique [8].

The auxiliary device could be used in another condition to make it also contribute in gain. It could even provide the same gain value introduced by the main device, if appropriate controlling its gate and drain voltages to assure,

$$\overline{Gm3_{eq}(t)}_{aux} \approx - \overline{Gm3_{eq}(t)}_{main}$$

$$\overline{Gm1_{eq}(t)}_{aux} \approx \overline{Gm1_{eq}(t)}_{main} \quad (6)$$

In Fig. 5, a plot of both *Pout* vs. *Pin* contributions in Eq. 6 are shown. The point where both HEMT's contribute with opposite IMDs is highlighted (*).

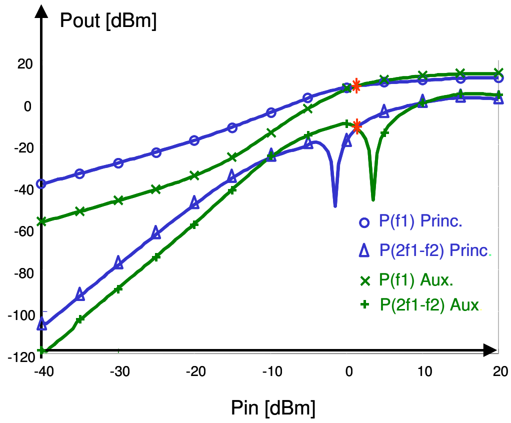

Fig. 5. Pout vs. Pin for the superposition connection.

IV. Active Antenna Implementation of Device-Level Linearization Techniques

The integration of active circuits and printed radiators has been receiving a lot of attention lately. The impedance characteristic of the antenna at the fundamental and higher harmonics as well as its capability for spatial power combining are being used in receiving and transmitting functions [10].

Both issues may also be employed when interested in improving a power amplifier linearity. In this paper, we will consider the possibility of implementing the derivative superposition technique in hybrid technology, using a dual feed antenna as in-phase power combiner.

In Fig. 6, a simplified diagram of the proposed transmitter front end is shown, where two in-phase NE3210s01 amplifiers are combined at the output using a dual excitation of a U shaped slot in an aperture coupled patch. Details about the structure and the reduction of the IMD radiated field component could be found in [11].

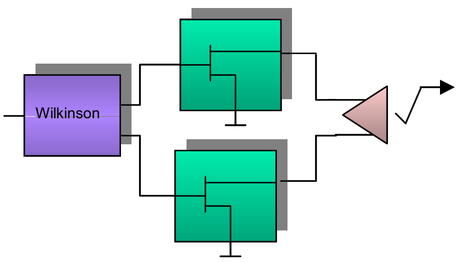

Fig. 6. Active antenna simplified diagram.

V. Conclusion

Some significant IMD characteristics of standard III-V FET's, either in small- or large-signal regimes have been summarized. These characteristics have been related to the conception of device-level linearization techniques, paying special attention to the particularities of large-signal operation. The power combining characteristic of some dual-feed antennas has been also introduced to produce a sort of highly integrated device-level linearization strategy. In all the cases, an accurate control of the device IMD performance has been shown to be required for developing low cost highly linear amplifiers.

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