NMOS SPDT Switch MMIC with >44 dB Isolation and 30 dBm IIP3 for Applications within GSM and UMTS bands.

P. Gould[1], J. Lin[2], O. Boric-Lubecke[2].

[1]Bell Laboratories, Lucent Technologies, Swindon, UK, SN5 6PP, pgould1@lucent.com
[2] Bell Laboratories, Lucent Technologies, Murray Hill, NJ, USA.

ABSTRACT

This paper describes the first reported, fully integrated, 0.25µm NMOS SPDT switch MMIC, for GSM and UMTS applications, fabricated on 10 Ωcm silicon substrate. This switch has the highest reported isolation, >44 dB below 2.2GHz, for a NMOS switch and high IIP3 (30 dBm at 900 MHz) for a 3V control voltage. Good RF port matches and <2.3 dB insertion loss are demonstrated over the whole frequency band.

INTRODUCTION

The increased high frequency response of sub-micron gate length NMOS devices has facilitated the design and fabrication of RF NMOS and BiCMOS transceiver MMICs for use in communication applications below 6 GHz. Although these technologies do not yet have the RF performance of GaAs, they do provide a very low cost fabrication route for chips used in high volume products. In order to reduce the cost of the RF front-end, individual chip cost and the overall component count must be reduced. This has encouraged many people to move towards "system on a chip" solutions. To realize such a goal, there is a need for high isolation, high linearity SPDT switch designs that can be fully integrated with other functional blocks in a MMIC form and require no additional external components. This paper describes the first fully integrated NMOS switch design that satisfies these criteria for GSM and UMTS applications, published to date.

To date little work has been published on analog SPDT switches using CMOS technology. Huang (1) describes a 900MHz SPDT switch, fabricated using 0.5 µm CMOS. This switch achieves an very good insertion loss of 0.8 dB, P(1dB) of 17 dBm and isolation >40 dB up to 1GHz. However, this is achieved by using three different DC control levels, one of which is 6Vand no data is given for port reflection coefficients.

Caverley (2) describes a 500 MHz SPDT switch, fabricated using 0.8 µm CMOS technology. This switch achieves 3dB insertion loss and >25 dB isolation at 1 GHz. The switch operates with a control voltage of 3.3 V. Titus et al (3) describes a BiCMOS transceiver front-end and includes a SPDT switch. This switch operates with a control voltage of 5V and a channel bias of 2.5V. An insertion loss of 1.3 dB and an isolation of 29 dB are achieved at 1GHz.

All the switches described within reference 1 to 3 require the off-chip DC blocking capacitors at RF input and output ports, if connected to other functional blocks that are not DC coupled. Without DC blocking capacitors the high linearity of this type of switch may not be achieved.

This paper describes the first reported fully integrated absorptive SPDT switch, fabricated using 0.25 µm NMOS on 10 Ωcm silicon substrate. This switch has a 30 pF on-chip DC blocking capacitor at each port and full on-chip matching to 50 Ohms. The switch has a port to port isolation of >44 dB below 2.2 GHz and IIP3 of 30 dBm and 27 dBm at 900 MHz and 1800 MHz respectively. This is the highest reported isolation for any NMOS SPDT switch reported to date. This paper shows the effect of on-chip DC blocking capacitors on the RF response of the circuit. A photograph of the SPDT NMOS switch is shown in Fig. 1. The chip has dimensions 1.5 mm by 1 mm.

DESIGN OF CMOS SPDT SWITCH

This switch was fabricated using 0.25 µm NMOS devices on a 10 Ωcm silicon substrate. Fig. 2 shows the circuit schematic for the switch. Port 1 is the common port and switching occurs between ports two and three by means of the control voltages, V1 and V2. When the switch has a low insertion loss state between ports one and two, V1 is set to 3V and V2 is set to 0V. These voltages are reversed for the low insertion loss path on the other pole of the switch. Voltage Vg, is normally 0V and but can be used to switch an extra 3 to 4 dB of attenuation into this path. This facility was included in the switch design to provide some gain control when used in a receiver chain. This is important for circuits that have tough linearity specifications and can be used to trade gain for higher IIP3. This switch design does not require any other bias voltages, has no DC current and can operate with voltages as low as 1.5V and OV with only a 0.3 dB drop in insertion loss at 900 MHz.

Inductors L1 to L4 are used to match the NMOS device capacitance parasitics to 50 Ohms, over the band 900 MHz to 2.2 GHz. It was found that series matching elements increased the achievable switch isolation, when compared to shunt LC matching by >20 dB in this band and also produced, due to the low Q, wider bandwidth matches at the ports. The inductors were fabricated using thick, 3 µm, top metal and wide conductors to minimize series resistance. The passive component values used within this design are shown in Table 1.

The active NMOS device size was chosen to give high isolation over the band 900 to 2200 MHz, while also maintaining a reasonably high P(1dB) and insertion loss of 1 to 2 dB. The device size was also chosen such that a small value series inductor of < 4 nH could be used to match the device to 50 Ohms. All the active devices used within this circuit, (T1-T6), are NMOS devices of size 48 x 0.32 µm x 3.6 µm. A multiple finger device structure was chosen to minimize source and drain parasitic resistance. Wide metal feeds, on M3 to M5, were used to access the device fingers to further reduce parasitic resistance. These metal layers were also chosen to minimize parasitic capacitance to substrate and drain to source capacitance in the OFF state that would degrade the isolation of the switch. Substrate guard rings with wide ground connections were used to isolate each device. Extraction of these parasitic elements from single device test structures has yielded values for parasitic source-drain capacitance of 30 fF and parasitic drain/source to substrate capacitance of <20 fF for each device. The substrate resistance in this state was found to be 30 Ω.

Because the SPDT switch was intended to be used within an integrated transceiver MMIC or “system on a chip”, a DC blocking capacitor was included at each port. Test structures of various DC blocks were analyzed and the 30 pF capacitor, equivalent circuit was de-embedded from the switch response, using the software simulation package HP ADS. The 30 pF capacitor used was made up of an array of 30 x 1uF capacitors. It had been found that this minimizes the series resistance of the capacitor. A larger capacitor was not chosen, as this would increase the capacitance to substrate parasitic and hence increase the insertion loss. The area of this capacitor was 42,780 μm^2. The equivalent circuit of this capacitor is shown in fig. 3.

MEASURED PERFORMANCE.

The measured isolation performance of the CMOS switch is shown in Fig. 3. RF on wafer (RFOW) measurement, in a 50 Ohm environment, shows a port to port isolation of 48 dB at 900 MHz, 52 dB at 1800 MHz and 44 dB at 2.2 GHz. This is the highest reported isolation for a NMOS SPDT switch MMIC reported to date.

Fig. 4 shows that that although the isolation is degraded by packaging., good isolation is still achieved within the SSOP-16 package. A packaged isolation of 42 dB is obtained at 900 MHz and 30 dB is achieved at 2.2 GHz. As no special improvements in test board design were employed to improve isolation, such as the use of shielded 50 ohm lines, these figures are comparable with those achieved from some commercial GaAs SPDT switches. F. Ndagijimana et al. (4) demonstrates a degradation in packaged switch isolation with increase in grounding inductance. The ground inductance of the SSOP-16 package is between 1 and 1.3 nH. From (4) this corresponds to about 10 dB decrease in isolation at 2.5 GHz due to the package, this agrees with our measurements at the high frequencies.

Compression measurements of the NMOS switch showed P(1dB) of 17.5 dBm and 18.5 dBm at 900 MHz and 1800 MHz respectively. Measurements of third order intermodulation products,

showed IIP3 of 30 dBm and 27 dBm at 900 MHz and 1800 MHz respectively. The insertion loss characteristic of the NMOS SPDT switch and the 30 pF DC blocking capacitor is shown in Fig. 5. This figure shows that each DC block adds 0.75 dB to the insertion loss to the RF path at 2.2 GHz. The insertion loss figure without the DC blocks, (normally quoted for switches) is 1.4 dB, 1.8 dB and 2.3 dB at 900 MHz, 1800 MHz and 2.2GHz respectively. Including the DC blocks degrades the insertion loss by 0.8 dB and 1.5 dB at 900 MHz and 2.2 GHz respectively. When the Vg control voltage is set to 3V, 3.2 dB attenuation is added to the RF path at 900 MHz and 4.2 dB attenuation is added at 2.2 GHz.

Fig. 6 shows the reflection coefficient at port 2. This measurement is typical of the other port responses, so only one graph is shown here. The reflection coefficient at port 2 is <-13 dB from 900 MHz to 2.2 GHz when the switch is in the high insertion loss state and <-14 dB when the switch is in the low insertion loss state.

CONCLUSION

The fully integrated NMOS switch presented here achieves >44 dB isolation and good linearity over the band 900 MHz to 2.2 GHz. Good RF port matches and <2.3 dB insertion loss have also been achieved over this frequency band. This NMOS switch MMIC demonstrates that a 0.25 μm CMOS process can be used to successfully integrate a fully matched SPDT switch and achieve a good isolation response on a 10 ohm.cm silicon substrate for GSM and UMTS applications.

ACKNOWLEDGEMENT

The author would like to thank Lucent Microelectronics for chip fabrication.

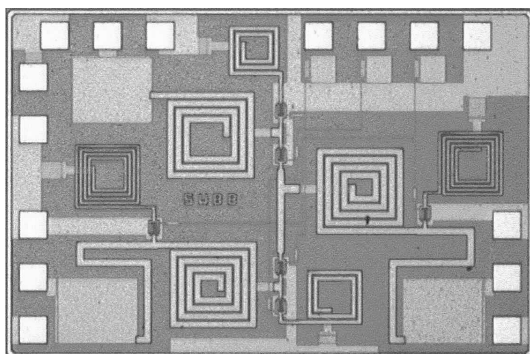
REFERENCES

[1] F. H. Huang, K.O, "A 900 MHz T/R switch with 0.8 dB insertion loss in a 0.5 μm CMOS process," *IEEE 2000 Custom Integrated Circuits Conference*. pp. 341-344.

[2] R. H. Caverly, "Linear and non-linear characteristics of the silicon CMOS monolithic 50-Ω microwave and RF control element," *IEEE Journal of Solid State Circuits*, vol. 34, No. 1, pp. 124-126, January 1999.

[3] W. Titus, M. Shifrin, V. Aparin, B. Bedard, "A silicon BiCMOS transceiver front-end MMIC covering 900 to 1800 MHz applications," *IEEE 1996 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest,* vol. 2, pp. 73-76.

[4] F. Ndagijimana, J. Engdahl, A. Ahmadouche, J. Chilo, "The inductive connection effects of a mounted SPDT in plastic SO8 package," *1993 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 91-94, June 1993.



1.5 mm x 1.0 mm

Fig.. 1 Die photo of SPDT CMOS switch.

C	30 pF	
R1	55 Ω	
R2	135 Ω	
L1	2.8 nH	Q=10.4
L2	3.3 nH	Q=10.3
L3	3.8 nH	Q=6.2
L4	0.8 nH	Q=5.9

Table. 1.Circuit component values of SPDT CMOS switch.

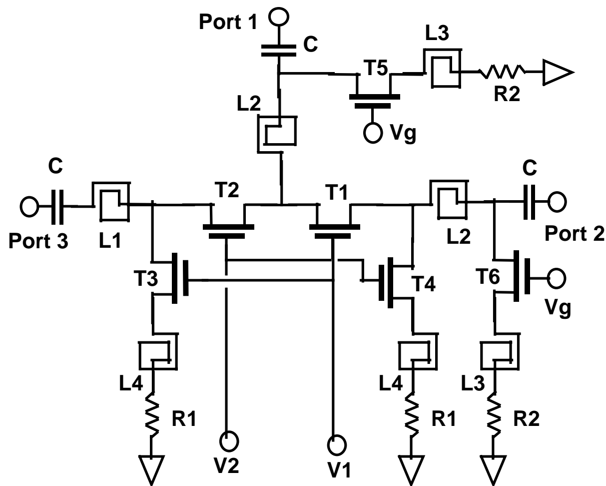


Fig. 2. Circuit schematic of SPDT NMOS switch.

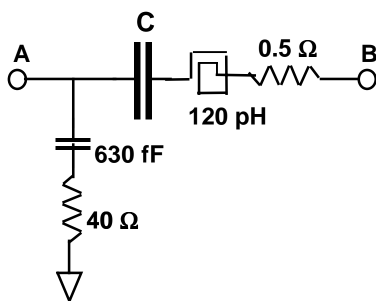


Fig. 3. Equivalent circuit of 30 pF DC blocking capacitor used in SPDT CMOS switch.

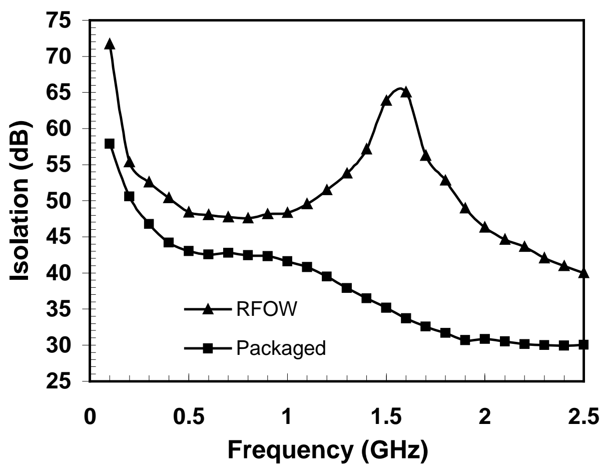


Fig. 4. Isolation of CMOS switch: RFOW measurement and SSOP-16 packaged measurement.

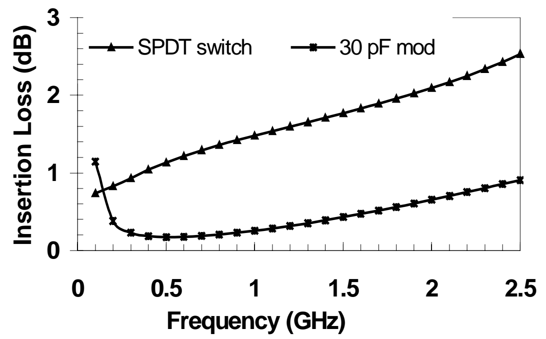


Fig. 5. The SPDT switch insertion loss response without DC blocking capacitors and insertion loss of one 30 pF DC blocking capacitor.

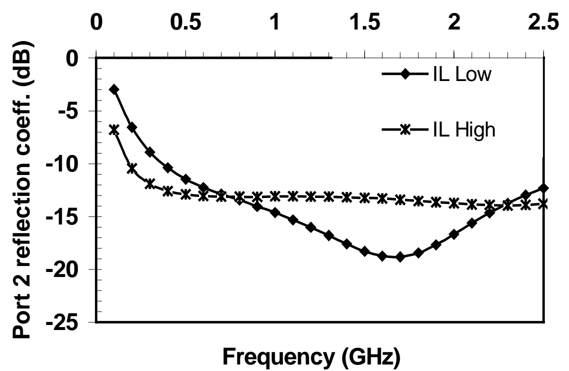


Fig. 6. Port 2 reflection Coefficient: Low insertion loss state (IL Low) and high insertion loss state (IL High).