A Balanced Sub-Harmonic Cold FET Mixer for 40GHz Communication Systems

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Abstract — **This paper reports a novel MMIC balanced sub-harmonic cold FET mixer for MVDS applications using 0.15mm GaAs pHEMT. The mixer, which includes a LO buffer amplifier, was optimized for highly linear up-conversion performance in the 42-43.5GHz RF band, 19.5-20.5GHz LO band and 2.45-3.45 GHz IF band. A dedicated simulation method has been developed to optimize conversion loss and determine optimum matching. To achieve better (2LO-to-RF) isolation a specific balanced architecture for sub-harmonic mixing has been elaborated. The first measurements of the fabricated MMIC circuit show 13,5dB conversion losses associated to high IF input power at 1dB compression of 15dBm, and (2LO-to-RF) rejection of 20dB in reasonable agreement with simulation results.**

I. Introduction

Emerging radio applications such as BWA (Broadband Wireless Access) and PtMP (Point to Multipoint) impose severe requirements on the output spectrum mask and on the linearity of the transmitters [1]. In order for these applications to succeed, high performance and low cost millimeter-wave circuits need to be developed. One of the critical components with regard to system performance is the up-converter mixer, which has the following key specifications :

- high linearity associated with low conversion losses. This enables to drive the IF port at high input power level while retaining linearity and to reduce the gain at the RF stage.
- strong output rejection of the unwanted mixing frequencies.

In order to achieve these goals, we investigated a novel balanced sub-harmonic mixer using cold FETs as the mixing elements [2].

II. Mixer Overview

The sub-harmonic mixing principle, which performs mixing using the second LO harmonic, shows better isolation properties than fundamental mixing, while requiring only half the LO frequency. To design a sub-harmonic mixer at millimeter-wave frequencies, an anti-parallel diode pair has typically been used [3]. The main limitation of diode resistive mixers comes from their relatively mediocre linearity. It has been demonstrated that cold FET mixers perform better in this domain [4]. In the cold FET configuration, the transistor gate is pumped by the LO signal, and the resulting time-varying conductance of the FET biased at Vds=0V is used to mix IF and RF signals, respectively applied and extracted from the drain of the source-grounded transistor.

In this study, the LO amplifier required to pump the mixer to a sufficient level is integrated on the same MMIC chip as the mixer to avoid the harmful influence of interconnections and to ensure maximal integration of the function, of which the block diagram is presented Fig. 1. The MMIC process used is a commercial 0.15mm power pHEMT process, which uses a 4mil GaAs substrate. The mixer was designed for the 42-43.5GHz RF band, 2.45-3.45GHz IF band and 19.5-20.5GHz LO band.

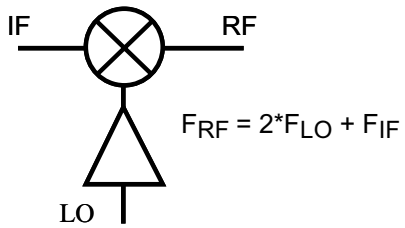

Fig. 1. Mixer block diagram.

III. Conversion Losses Optimization

In order to minimize conversion losses, it is necessary to match IF and RF ports to their optimal values. The goal of the proposed methodology is to enable the simulation of the optimal IF and RF impedances with regard to conversion losses.

Mixers are inherently 3-port non-linear devices. However, for a small input signal, it is possible to consider the mixer, pumped at a given LO level, as a quasi-linear system [5] between its input and output ports (Fig. 2). The method we have implemented consists in determining the admittance matrix of the pumped mixer between the IF and RF ports at the corresponding frequencies. The well-known equations for linear 2-port systems [6] can then be applied to determine the optimal IF and RF impedances, as well as the associated conversion losses. Two tone harmonic balance simulations have validated the obtained results. The main interest of this method, which can easily be implemented in any commercial simulator, is that it enables research of the optimal working conditions of the mixer and thus

optimization of the conversion losses. It has been applied to assess the potentialities of several MMIC foundry processes for the cold FET sub-harmonic mixer application. Several points have been observed :

- The mixer gate bias must be very negative, well below pinch-off.
- Conversion losses are relatively high.
- The optimal impedances are generally very different from 50Ω. Device size should be chosen so as to facilitate matching.
- The gate input impedance at the LO has a strong reactive part and thus is difficult to match .
- Conversion losses increase very strongly if the mixer is not sufficiently pumped. An optimal pump level exists.
- The performance achieved is very sensitive to the input and output loads at the spurious frequencies [7]. Of course, the output load at the LO fundamental is of particular importance.

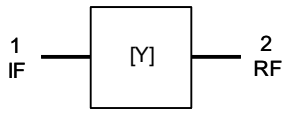

Fig. 2. Quasi-linear matrix of the pumped mixer.

The proposed simulation method is general: It can be applied similarly to a single transistor, or to a partially or even fully completed mixer. Seeing that the method is applied to the transistor with its first input/output matching networks, the loads seen by the transistors at the spurious frequencies approach their final values and thus the obtained results tend towards the final performances.

IV. Circuit Architecture

To obtain a sufficient output suppression of the unwanted 2LO frequency, it is necessary to use a balanced topology because the 2LO frequency is too close to the pass-band to be filtered by other means. The principle of a balanced structure is to use the phase differences between two identical active devices working under the same conditions to enable in-phase combination or cancellation of the different frequencies at the output. In the case of this sub-harmonic mixer, the structure uses a Lange coupler at the LO input and a 180° balun at the IF input (Fig. 3). This structure is not naturally balanced because it does not include a balun at the input. The output phase difference at the mixing frequency m*LO+n*IF is given by m*90°+n*180°. This means the two transistors see different output loads at the critical LO frequency, thus they do not operate under the same conditions, and as a consequence the structure does not provide the desired phasing relations. To solve this problem two solutions theoretically exist : to short circuit the LO frequency directly at the output of the transistors, or to short circuit it at the middle of the output structure to create a virtual ground. In practice, a combination of these two methods must be used to achieve balanced operation by integrating three λ/4 open stubs at the LO frequency (Fig. 4).

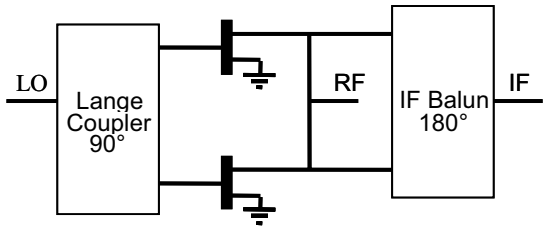

Fig. 3. Structure of the balanced mixer.

In addition, the RF frequency is blocked on the IF paths by a λ/4 line followed by a λ/4 open stub at the RF frequency, while MIM capacitors block the IF frequency on the output RF path (Fig. 4). The lengths of the different stubs must be adjusted so as to ensure proper mixer operation for the given LO and RF bands. Special care was devoted to the design of the transistor output network because it has a critical influence on mixer performance.

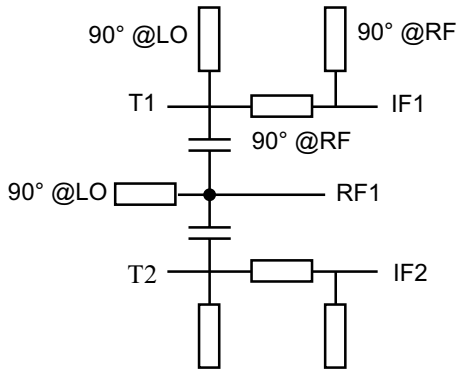

Fig. 4. Transistor output network.

To ensure maximum integration of the mixer, it was decided to integrate the IF balun on-chip. However, given the low IF frequency, on-chip distributed balun would have occupied too much GaAs real estate, so a lumped element balun was used instead (Fig. 5) [8].

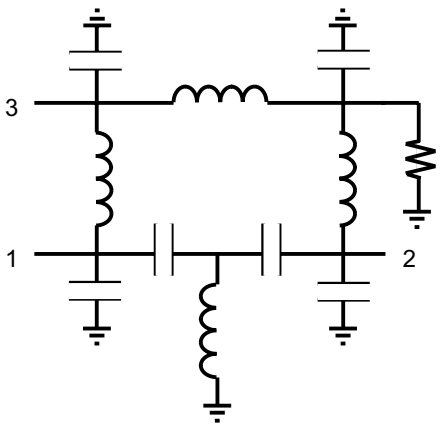

Fig. 5. Lumped element 180° hybrid.

Electromagnetic simulations were used to simulate the 20GHz Lange coupler and to take into account all coupling and discontinuity effects in lines. The 50Ω Lange coupler properties ensures a good separation between the mixer and the LO buffer amplifier and thus enables them to be designed separately. Fig. 6 shows the photograph of the fabricated mixer, whose dimensions are 3.35*2.2mm.

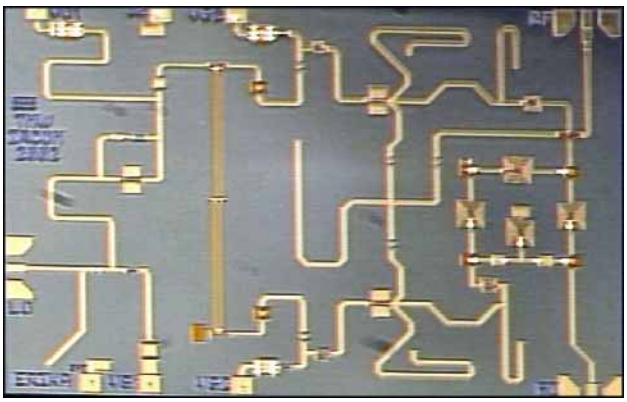

Fig. 6. Photograph of the fabricated mixer.

V. Simulated And Measured Performance

The hot and cold non-linear models of the 2x75µm transistor, used respectively for the amplifier and the mixer design, were extracted at IRCOM from pulsed on-wafer I/V and [S] parameters measurements in the 2-40GHz band.

The integrated LO buffer consists in a single-transistor saturated feedback amplifier. While biased at Vds=2.3V, it delivers 12dBm output power (the optimal pump level for the mixer) for a fixed input power of 5dBm. The output power can be adjusted if necessary by varying the drain bias. The saturated mode of operation and the resistive feedback topology were selected so as to minimize the influence of thermal effects on the amplifier output power.

The mixer was measured in a test-fixture with the two cold FETs biased at Vgs=-2.4V for F_{LO}=20GHz. Conversion losses are plotted versus IF frequency (Fig. 7). Small-signal conversion losses of 13.5dB are obtained, while the IF input power at 1dB compression reaches 15dBm. 2LO output rejection performances are given Fig. 8, a 2LO-RF rejection of 20dB is achieved. In addition, IF and RF return losses better than 10dB are obtained. Table 1, which recapitulates measured and simulated performance shows that measured results are in reasonable agreement with simulation. Moreover, retro-simulations show that imperfect IF balun operation could account for the slightly degraded fabricated mixer performance.

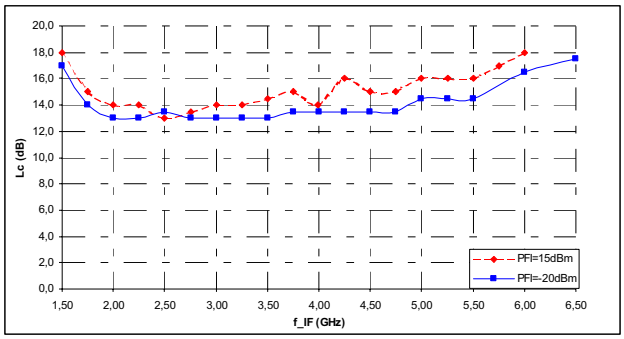

Fig. 7. Measured conversion losses vs. IF frequency for -20dBm and 15dBm IF input power, F_{LO}=20GHz.

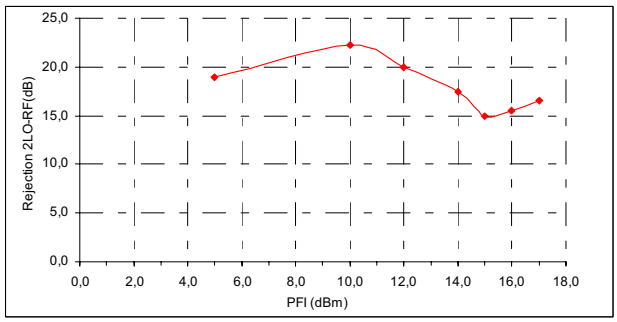

Fig. 8. Measured 2LO-RF rejection vs. IF power, F_{LO}=20GHz, F_{IF}=3GHz.

Results	Simulation	Measurements
Conversion Loss (Lc)	13.5 dB	13.5 dB
Input Power @1dB compression	>15 dBm	15 dBm
2LO-RF Rejection	25 dB	20 dB
Input-Output Return Loss	> 10 dB	> 10 dB

TABLE I
Comparison of Simulated and Measured Results.

VI. Conclusion

This paper reports the design of a balanced sub-harmonic MMIC mixer using cold FETs. The balanced structure is composed of a Lange coupler at the LO input and a lumped element 180° balun at the IF input. A LO buffer amplifier is integrated on-chip so as to enable optimal mixer operation for 5dBm LO power. The first measurements of the fabricated circuit show promising performance : for F_{LO}=20GHz, upper side band conversion losses of 13.5dB are obtained with high IF input power at 1dB compression of 15dBm and 2LO-to-RF rejection of 20dB.

Acknowledgement

This work has been supported under the European research project PIDEA n° 99122.

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