# High Performance 50nm T-Gate $In_{0.52}A1_{0.48}As/In_{0.53}Ga_{0.47}As$ Metamorphic High Electron Mobility Transistors

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*ABSTRACT* — **We report the performance of 50 nm gate length metamorphic GaAs HEMTs with maximum transconductance($g_m$) of 1200 mS/mm and current cut-off frequency($f_T$) of 300 GHz. The devices were fabricated with a novel UVIII/PMMA T-gate resist stack and a non-selective "digital" wet etch gate recess technology which results in a highly uniform, high yield sub-100 nm HEMT technology.**

## I. INTRODUCTION

InP based InGaAs/InAlAs High Electron Mobility Transistors (HEMTs) are considered to be one of the most promising devices for next generation millimeter wave and optical communications because of their superior high frequency and low noise performance. Relative to GaAs however, InP substrates are more expensive and brittle, raising issues of economies of scale and yield. These obstacles can be overcome by implementing a buffer technology that allows the use of GaAs substrates to grow structures lattice matched to InP – the metamorphic GaAs HEMT technology.

For millimetre-wave performance beyond 100 GHz, it is essential to reduce the gate length of HEMT devices. The main challenge to realize short gate length devices is the electron-beam lithography technology for T-gate fabrication and the recess technology to remove the heavily doped cap layer. Conventional electron-beam lithography T-gate fabrication is commonly based on PMMA and related co-polymers[1,2]. In such resist stacks there is a relatively limited difference in the electron beam sensitivity of the resists and this limits the ultimate cross-sectional dimensions of the T-gates [3]. In contrast, UVIII is a Shipley DUV photoresist, which is almost five times more sensitive to electron beam exposure than PMMA thus enabling ultra-short footprint T-gates with larger cross sectional areas to be written at higher speeds [4]. The increased cross-sectional area of the gate results in reduced DC and RF resistance/inductance of the gate electrodes giving the highest performance mm-wave devices.

Gate recess etching is another challenge for the realization of short gate length devices because the gate recess structure fundamentally determines both performance and uniformity of devices. In our previous work, we developed a novel high uniformity, highly reproducible non-selective wet digital gate recess etch process for 120nm gate length InP HEMTs.[5] In this paper, we successfully implement this technology at the 50nm technology node.

## II. MATERIAL STRUCTURE AND DEVICE FABRICATION

The layer structure of the devices reported this work was grown in-house by molecular beam epitaxy (MBE) on a 3 inch diameter (100) GaAs substrate. The epilayer was grown on a strain relief buffer designed to allow the growth of material normally grown lattice-matched to InP on to a GaAs substrate. The buffer consists of a sequence of six steps of InAlAs 0.2 μm thick with the In content increasing from 0% to 53%. The growth conditions have been optimised to increase the mobility of the indium adatoms and so reduce the surface undulations normally associated with these strain relief buffers. A superlattice is used before the growth of the InGaAs channel to ensure a smooth inverted interface and to reduce the density of dislocations in the device epilayer. The room-temperature epi-layer properties were measured using Van der Pauw structures giving room temperature sheet density of $9.6\times10^{12}$ $cm^{-2}$ and mobility of 5300 $cm^2/Vs$. After processing and wet etch removal of the InGaAs cap room temperature sheet density of $3.6\times10^{12}$ $cm^{-2}$ and mobility of 7800 $cm^2/Vs$ were measured.

The 50nm HEMTs devices were realized using the in-house MMIC fabrication process. Ni-Ge-Au based ohmic

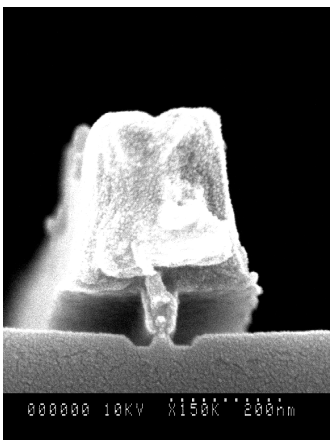
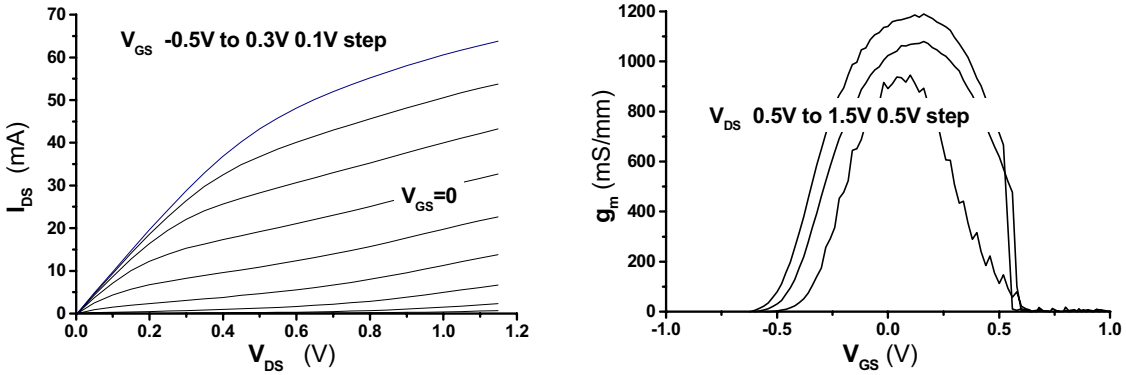



Figure 1 SEM image of the cross section of a fabricated T-gate from a real device.




(a) I-V characteristics

(b) $g_m$ characteristics

Figure 2 Extrinsic DC output characteristics of 2x50 µm 50 nm GaAs MMHEMT

contacts were annealed at 280°C using rapid thermal annealing, resulting in transistors with repeatable ohmic contact resistances around 0.08 Ω·mm. Wet-etch mesa isolation was performed using a 1:1:100 phosphoric acid:hydrogen peroxide:water solution. The 50 nm T-gates were realized by electron beam lithography (Leica Microsystems Lithography LTD EBPG-5HR 100) utilizing a UVIII/PMMA resist stack [4]. Gate recess etching was performed using non-selective wet digital gate recess etch process[5]. Schottky gate metallisation was Ti-Pd-Au. Bond pad metallisation of 400nm Au was used to facilitate electrical connection to the devices. A selection of two finger devices with widths in the range 25-75 µm were fabricated in coplanar waveguide technology, to facilitate direct on-wafer mm-wave characterization.

Figure 1 shows scanning electron microscope (SEM) image of the cross section of a fabricated T-gate taken from a real device. It clearly shows that a gate recess width of 30 nm each side of the gate was achieved.

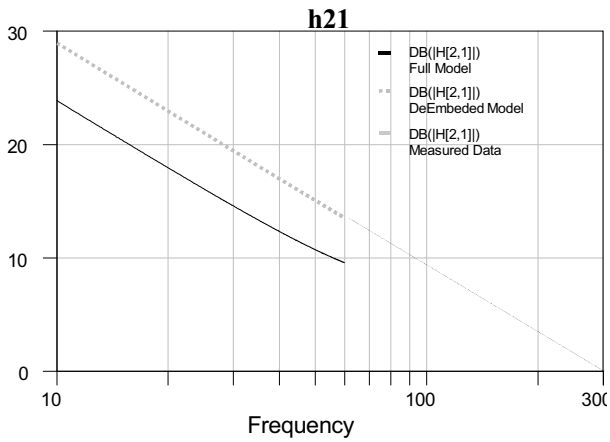



Figure 3 Measured and modeled $|h_{21}|$ against frequency

## III. DEVICE PERFOMANCE

The I-V and $g_m$ characteristics of the devices are shown in figure 2

A $g_m$ of 1100 mS/mm was achieved from most of the devices at drain source bias of 1.2 V. The best performance devices showed a $g_m$ of 1200 mS/mm at drain source bias of 1.5 V.

On-wafer S-parameter measurements were performed from 0.04-60 GHz over the full bias range, using an Anritsu 360B Vector Network Analyser fitted with on-wafter Picoprobes from GGB. Calibration was performed using Cascade Microtech's Impedance Standard Substrate (ISS) and the LRRM technique. FET model extraction was performed at each bias point to study the performance. Figure 3 shows a plot of measured and modeled $|h_{21}|$ against frequency for a 2×50 µm gate width device biased at $V_{ds}$=1.2V, $V_{gs}$=0V. At this bias, using –20dB/decade rolloff, the device has an extrapolated peak $f_T$ of 300 GHz .

The mechanical gate yield on 12mm by 12mm samples containing 112 devices, which mainly depends on gate lithography and gate recess etching, was 99%. The DC and microwave performance yield were 95% for 2×25 µm gate width devices and 90% for 2×50 µm devices.

## IV. CONCLUSIJON

In conclusion, we report the fabrication of 50nm GaAs metamorphic HEMT devices using UVIII/PMMA T-gate bilayer resist stack and a non-selective "digital" wet etch gate recess technology. Initial measurement results show very promising performance in both DC and mm-wave with an $g_m$ of 1200 mS/mm and $f_T$ of 300 GHz obtained from a 2×50 µm gate width device. In conclusion, the combination of UVIII/PMMA T-gate e-

beam lithograph and "digital" wet etch gate recess technologies offer significant process latitude which result in high yield, highly uniform device characteristics, which in combination with the device performance, suggests this will be suitable to the realization of very high performance MMICs for applications beyond 100 GHz. Work is ongoing to further optimize device layer structure and fabrication procedures to improve both the DC and RF performance.

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