20 Gbit/s Decision Feedback Loop for Optical Communications

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Abstract — **A new concept for a high-speed data decision with a feedback loop for cancellation of intersymbol interferences (ISI) is proposed. Operation up to over 20 Gbit/s has been measured. The improved speed performance has been obtained by a new concept merging the parallel principle and a twin DC references approach.**

I. INTRODUCTION

Electrical filter concepts for mitigation of intersymbol interference at 10 Gbit/s and above, e.g. caused by polarization mode dispersion, can be roughly subdivided into feedback filters and transversal filters [1].

The basic idea behind decision feedback loop (DFL) is to subtract the ISI from a certain bit before the decision in the subsequent block. The ISI, in turn, is estimated based on the knowledge about the decision of the predecessor bit. In a straightforward manner, this principle can be implemented by feeding back the predecessor bit with a certain weight and subtracting this signal from the successor bit before its decision. The first decision feedback loop capable of operation at 10 Gbit/s was reported in [2]. The speed performance of this concept is, however, limited by the finite delay of the feedback loop. To overcome this drawback, the use of two DC references, which correspond to the feedback signals for a preceded "0" and "1", respectively, has been proposed in [3]. Merging this concept with the parallel approach [4] enables operation at 20 Gbit/s and above. Details of circuit design, technology, and measured results will be given in the following.

II. CIRCUIT DESIGN AND REALIZATION

Figure 1 shows the principle block diagram of the parallel data decision with feedback loop. Data, clock as well as references are complementary signals, but are drawn as single-phase signals for simplification. The circuit contains two parallel decision branches, which are triggered by rising edge and falling edge of $f/2$ clock, respectively.

Two comparators with complementary DC references V_{ref} and $-V_{ref}$ are in front of each branch. V_{ref} corresponds to a predecessor bit '1' while $-V_{ref}$ corresponds to "0". The current bit is decided in respect of both references simultaneously and latched in parallel paths. In fact, complementary data inputs are fed to a differential amplifier, which is accordingly tilted by the reference

voltages applied to a second differential pair working on the same loads. It shall be emphasized that both decisions are performed without waiting for the predecessor decision results. The references can be externally adjusted to the actual ISI. Finally the decision result of one of the paths will be selected by a 2:1 selector according to the predecessor bit.
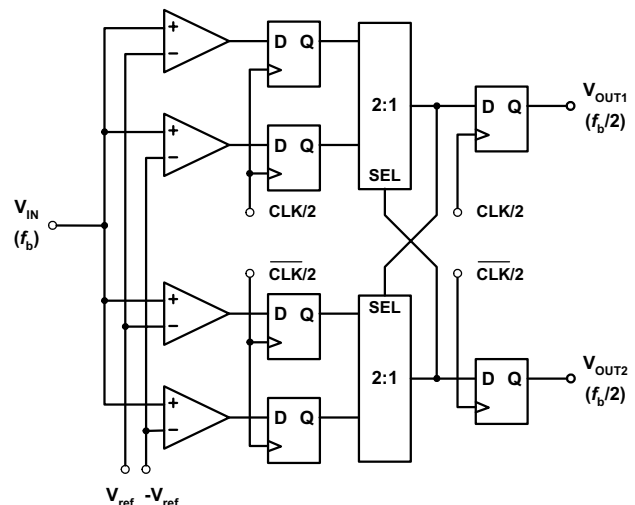

Fig. 1.   Principle block diagram of the circuit

Note that this predecessor bit comes from the other decision branch due to the parallel decision approach. However, the final latch has to be kept out of this feedback loop to meet the loop delay requirements. Nevertheless, the circuit is stable and no oscillation will occur. To understand this we have to envision that a preceding "1" can only increase the level of the succeeding bit, while a preceding "0" can only reduce its level due to the physics of ISI. Thus, only a positive V_{ref} is reasonable from the physical point of view, or by other words $V_{ref} > -V_{ref}$ will be always fulfilled. This means, that the conditions $V_{IN} > V_{ref}$ and $V_{IN} < -V_{ref}$ can never be fulfilled simultaneously. Finally, one can easily prove, that the loop is stable for all other cases.

III. MEASURED RESULTS

The OMMIC ED02AH process, i.e. an enhancement-depletion AlGaAs/GaAs HEMT technology with 0.2 μm gate-length and an f_T of about 60 GHz, was used to

fabricate the chip. The circuit was realized in SCFL (Source Coupled FET Logic) for better common-mode noise rejection and high-speed operation. Differential coplanar waveguides and termination resistors have been implemented on chip for both clock and data signals. The die photograph is shown in Fig. 2. The whole circuit comprises 310 FETs and occupies 2.5-mm^2 chip area including the pads.
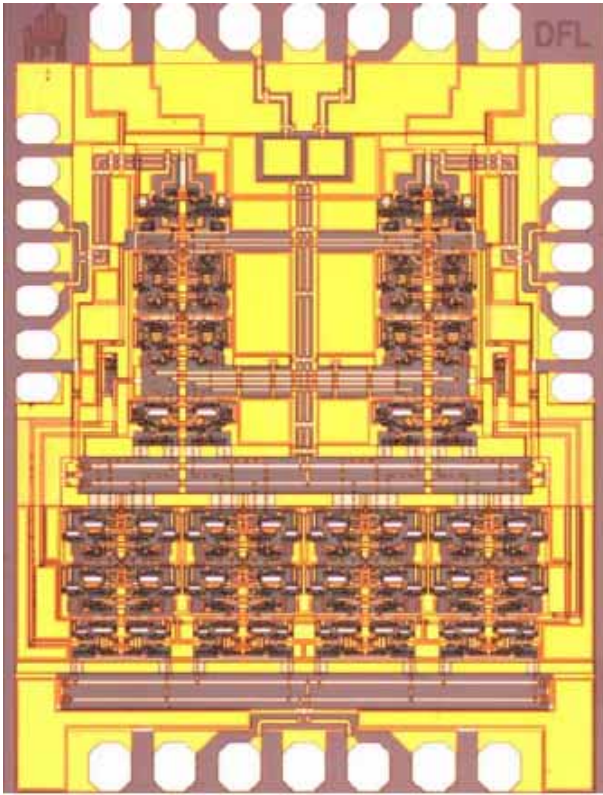

Fig. 2.   Die photograph of DFL

While the ISI cancellation function has been demonstrated in [5], the maximum operating speed of DFL was tested in normal parallel decision mode by setting the two reference voltages to balance state. Although the feedback loop in this case will have no influence any more on the results of decision, since the two inputs of each selector are identical, the timing conditions within the feedback loop can still be verified.
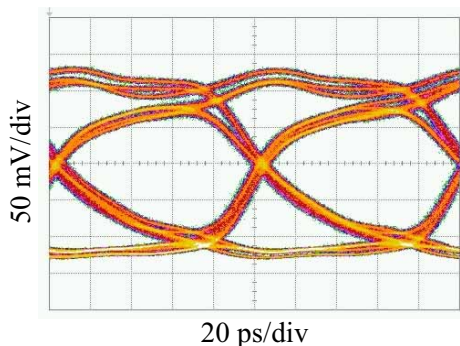

Fig. 3.   Output eye diagram at 20 Gbit/s

The measurement was performed on-wafer using four P-G-S-G-S-G-P (P: Power, G: Ground, S: Signal) 50 Ω coplanar probes. Dual power supplies (+2.0 V and -3.0 V) were used to allow a bias-free data input. Correct data decision has been obtained up to 24.5 Gbit/s bit rate with $0.2V_{p-p}$ PRBS (2^4-1) data inputs and about 1.8 W of power consumption. The output eye diagram at 20 Gbit/s data inputs is shown in Fig. 3. A phase margin of 25 ps (90 degree for $f/2$ clock) at this data rate was measured.

IV. CONCLUSION

The design, fabrication and measurement results of a high-speed data decision with a feedback loop for cancellation of ISI were presented. The decision IC fabricated with 0.2 μm gate-length AlGaAs/GaAs HEMTs exhibits an operation above 20 Gbit/s, while consuming 1.8 W of power.

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