Advanced III-V HEMT MMIC Technologies for Millimetre-Wave Applications

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***Abstract* — In this paper, we review advanced III-V HEMT device technologies for millimetre-wave applications, particularly targeted above 100 GHz. We demonstrate performance advantages in moving to self-aligned T-gate strategies in lattice matched InP HEMTs. For 120 nm gate lengths, we have obtained self-aligned, non-annealed Ohmic contact devices with g_m of 1450 mS/mm, f_T of 220 GHz and f_{max} of 435 GHz. We will also present data on a high yield 50 nm T-gate process in the metamorphic GaAs material system utilizing non-selective digital wet etching with performance metrics including g_m of 1500 mS/mm and f_T of 350 GHz, to our knowledge, the fastest GaAs-based transistors reported to date.**

I. INTRODUCTION

There has been renewed interest recently in the realization of scaled sub-100 nm III-V HEMTs with ultimate applicability in a wide range of communication, imaging and sensing applications beyond 100 GHz [1-2]. In this paper, we will review recent technological developments at the University of Glasgow, leading to the realization of advanced III-V HEMTs for MMIC applications beyond 100 GHz. The emphasis of the paper is on developing robust technology and process modules which are transferable between a range of material systems, enabling the demonstration of scaled, high performance III-V HEMTs.

II. SCALED III-V HEMTS

A. Self-aligned 120 nm lattice matched InP HEMTs

To fully exploit the intrinsic performance of advanced III-V HEMTs, it is vital that parasitic device elements such as source and drain resistance are minimized. Such parasitic resistances can be minimized by introducing a self-aligned gate process, in which the separation of the source and drain contacts are defined by the geometry of the low resistance T-gate.

In moving to a self-aligned process however, a number of technological challenges have to be overcome including the ability to form thin, low resistance Ohmic contacts.

A self-aligned T-gate process a cross section of which is shown in Fig. 1, has been developed [3-4], which when combined with a double delta-doped InGaAs/InAlAs lattice matched HEMT vertical architecture [5], results in a thin, non-annealed Ohmic contact process optimized to minimize the access resistance from the metal contact to the device channel.

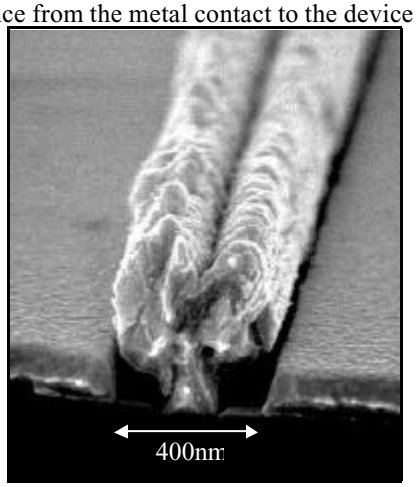


Fig. 1 - SEM image of a self-aligned 120nm T-gate.

Using the process flow described in [3], 120 nm gate length self-aligned Ohmic contact lattice matched InGaAs/InAlAs HEMTs were fabricated and compared with identical geometry "regular" non-self aligned devices with a 1.6 ?m source drain separation.

Fig. 2 compares the DC transfer characteristics of the two device types, clearly showing a reduced low field resistance in the self-aligned devices.

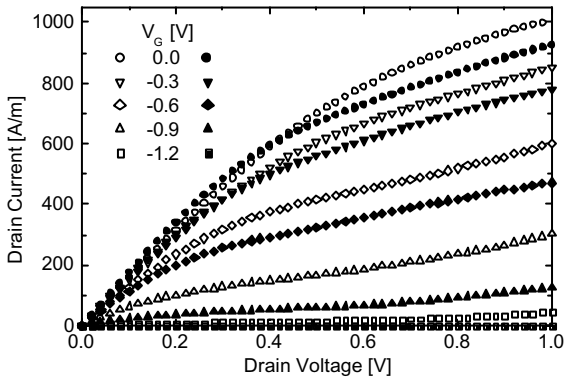


Fig 2. $I_{ds}(V_{ds},V_{gs})$ plots for "regular" (transparent) and self-aligned (filled) 120nm gate length devices

Fig. 3 compares the $g_m(V_{gs})$ characteristics of the "regular" and self-aligned devices, showing the enhancement in transconductance arising from moving to a self-aligned strategy. Fig. 4 show the h_{21} plot for the "regular" and self-aligned devices respectively. From the measured S-

parameter data, f_{max} of 435 GHz and 360 GHz have been extracted for the self-aligned and "regular" devices respectively.

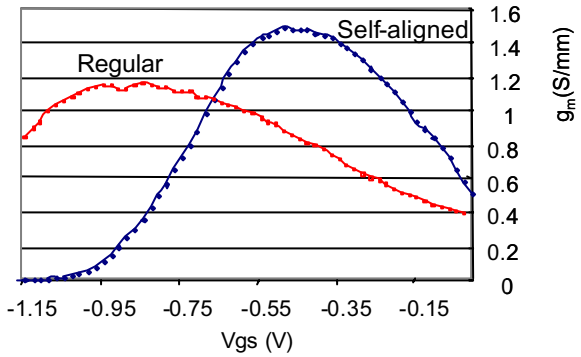


Fig 3. Comparison of g_n of "Regular" and self-aligned 120 nm gate length devices

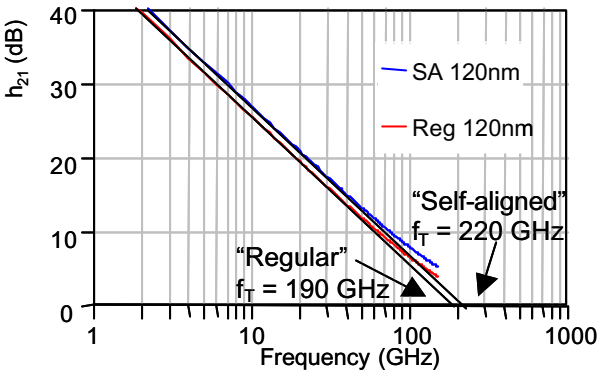


Fig 4. Comparison of f_T of "Regular" and self-aligned 120 nm gate length devices

Clearly, these devices have performance metrics which made them attractive candidates for MMIC applications beyond 100 GHz. In addition, we have similar devices, scaled for the 70 nm technology node, which will be reported at a later date.

B. 50nm GaAs mHEMTs

As has been shown above, high indium concentration channels are the vehicle to the realization of HEMTs for applications beyond 100 GHz. However, few foundries are well equipped for handling InP substrates due to the relative brittleness of the substrate, and in addition, the economies of scale of working with 150 mm diameter wafers are not accessible to InP-based devices.

For these reasons, many groups have been actively pursuing the metamorphic GaAs HEMT solution (GaAs mHEMTs), which offers "InP-like" performance on a GaAs substrate.

In the second part of this paper, we present a high-yield 50 nm metamorphic GaAs HEMT technology based on non-selective "digital" wet chemical etching with performance metrics which suggest this technology is applicable to MMIC applications beyond 100 GHz. In addition, the process developed has proven to be high yield, and highly uniform.

The process flow for the realization of 50 nm T-gate devices utilizing a non-selective "digital" etching technology has been described in detail elsewhere [6-8].

Fig. 5 shows a cross-section of a 50 nm T-gate device in a gate recess trench formed by "digital" etching.

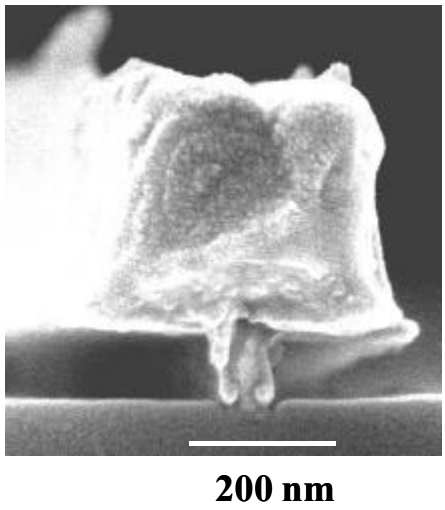


Fig 5 - SEM image of a 50 nm GaAs mHEMT.

Fig. 6 shows the DC transfer characteristics of a typical 50 nm GaAs mHEMT, whilst Fig. 7 shows the transconductance of these devices.

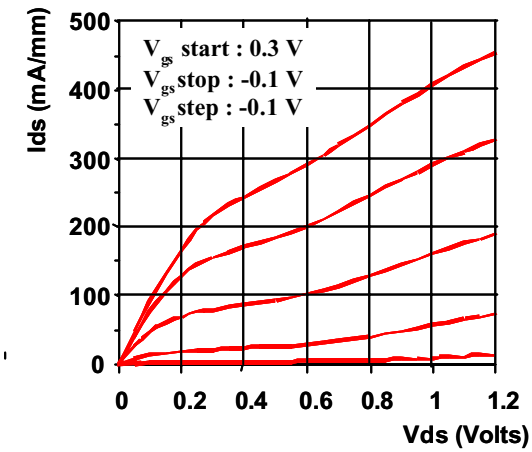


Fig 6. Typical $I_{ds}(V_{ds},V_{gs})$ plot of 50 nm gate length GaAs mHEMT technology

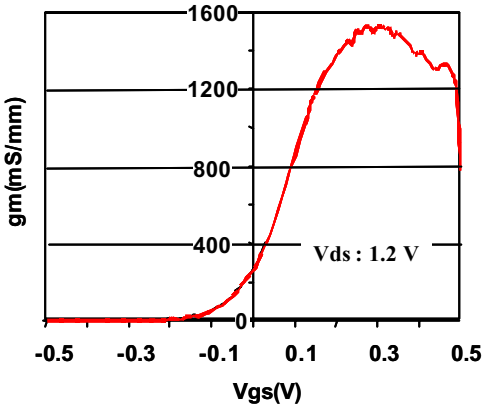


Fig 7. Typical $g_m(V_{gs})$ plot of 50 nm gate length GaAs mHEMT technology

To assess the yield and uniformity of the "digital" gate recess etching process, a sample of 54 devices were characterized across a wafer fabricated using the process described in [7].

The functional yield was 96%, with a mean and standard deviation I_{dss} of 569 mA/mm and 40 mA/mm respectively, as shown in Fig. 8. This translates into a threshold voltage uniformity of around 60mV.

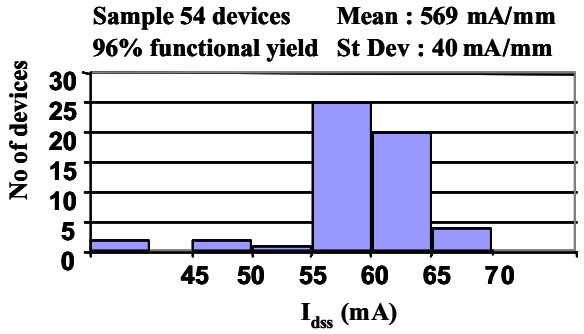
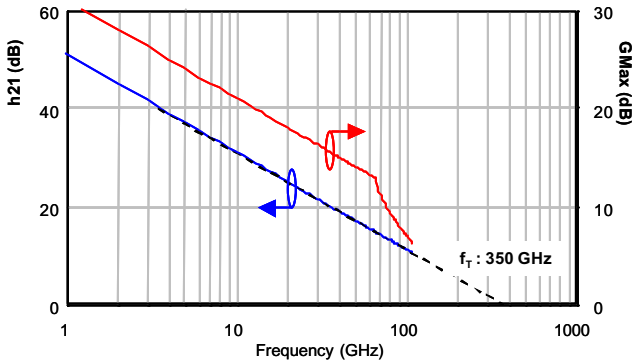


Fig 8. Spread of I_{dss} on sample of 50 nm GaAs mHEMTs

Fig. 9 shows the h_{21} and G_{max} plots for a typical 2x25mm device, which shows an f_T of 350 GHz and 16 dB gain at 100 GHz.

Fig 9. h_{21} and G_{max} for typical 2x25? m 50 nm GaAs mHEMTs



These performance metrics, together with the yield data presented in Fig. 8, suggests that this 50 nm GaAs mHEMT technology is also highly attractive for MMIC applications beyond 100 GHz.

III. Conclusion

In this work, we have presented a number of process modules which, in combination with advanced III-V HEMT growth techniques, result in lattice matched InP HEMTs and metamorphic GaAs HEMTs with gate lengths in the range 50 – 120 nm which are well suited to the realization of MMICs for applications beyond 100 GHz. By utilizing self-aligned gate strategies, significant performance advantages at the 120 nm technology node can be obtained for lattice matched InP HEMTs.

By exploiting non-selective wet chemical "digital" gate recessing technologies, high yield, high uniformity GaAs mHEMTs can be realized at the 50 nm technology node.

Both these HEMT technologies, and other sub-100nm device processes under development in Glasgow, will enable the realization of MMICs for applications beyond 100 GHz.

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