

InP HEMTs and HBVs for Low Noise and Ultra-High Speed: Device and Circuit Research at Chalmers University of Technology

Herbert Zirath, Jan Grahn, Niklas Rorsman,
Anders Mellberg, Jan Stake, Ilcho Angelov and Piotr Starski

Chalmers University of Technology, Microwave Electronics Laboratory, MC2, SE-412 96, Göteborg, Sweden

Abstract — An overview is given of the Chalmers research activities in InP-based devices and circuits for very high-speed and low noise applications. Both InP HEMTs and circuit implementations are presented including 50 nm gate length devices and analog MMICs at F-band and W-band. We also present results from research on extremely low-noise InP HEMT amplifiers for cryogenic applications and HBV devices for THz generation.

I. INTRODUCTION

Devices based on InP such as heterojunction bipolar transistors (HBTs), high electron mobility transistors (HEMTs) and heterostructure barrier varactors (HBVs) represent the fastest semiconductor technology today. The InAlAs/InGaAs HEMT grown on semi-insulating InP has been demonstrated with f_T of 562 GHz [1] and f_{max} of 600 GHz [2]. Potential applications are found in satellite communication systems, remote sensing and wireless LAN [3]. HEMT-based circuits for low-noise signal amplification have been demonstrated up to 215 GHz [4]. The high f_T of InP HEMTs also makes it particularly attractive for digital systems; Recently, switching at 100 Gbps was demonstrated [5]. Even though the InP HEMT technology recently has been challenged by corresponding structures on GaAs substrates [6], *i.e.* the so-called metamorphic approach, the highest f_T and f_{max} are still found for the devices grown on InP bulk.

At Chalmers University of Technology in Göteborg, Sweden, activities on InP based devices have been ongoing for around ten years. In this paper, an overview is presented of the research carried out for InP HEMTs and HBVs primarily focused on very high-frequency applications > 100 GHz or extremely low noise amplifiers.

II. DEVICE TECHNOLOGIES

A. 50 nm InP HEMTs

At Chalmers, we have recently developed InP-based HEMTs with 50 nm gate length using a new electron beam lithography tool, the 9300 JEOL tool. The epitaxial stack consists of a pseudomorphic structure with a 65% In-containing channel about 150 Å thick. In Fig. 1, a SEM micrograph is shown for a mushroom-shaped HEMT gate as defined by a single exposure in a PMMA-

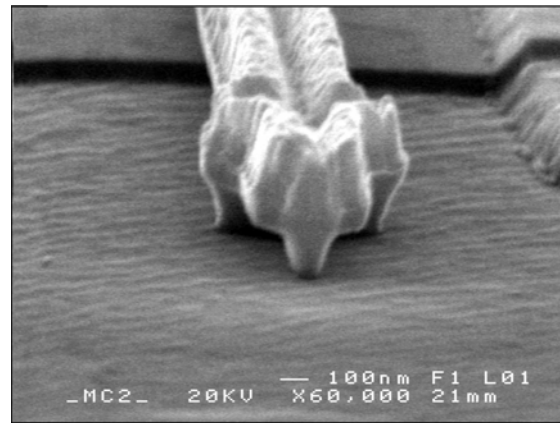


Fig. 1. SEM micrograph of the gate in the Chalmers InP HEMT process.

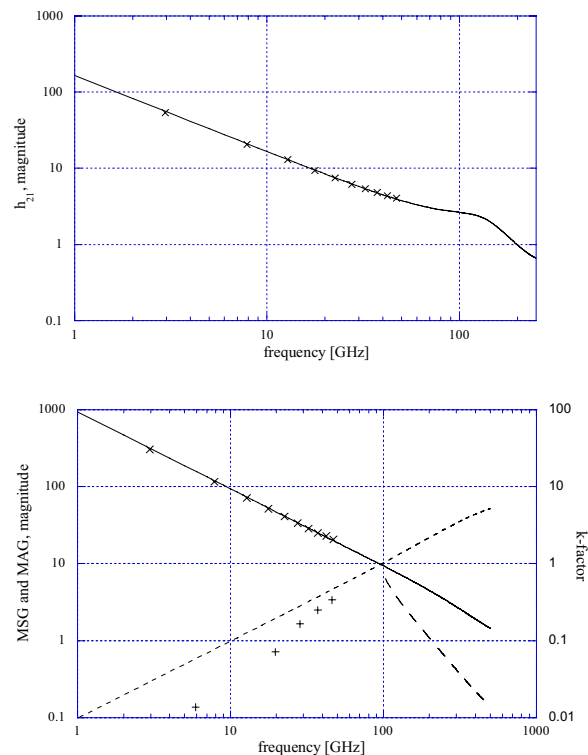


Fig. 2. HF characteristics of the 50 nm InP HEMT: Measured (\times) (as calculated from s-parameters) and modeled (line) (from equivalent circuit) h_{21} vs. frequency, and measured (\times) and modeled (line) MSG, modeled (---) MAG, and measured (+) and modeled (---) k-factor vs. frequency.

COPOLYMER resist combination. The device intrinsic transconductance is 1250 mS/mm.

The high-frequency device characteristics for the 50 nm device under a bias of $V_{DS} = 1$ V are plotted in Fig. 2. The extrapolated f_T from measured s-parameters ($h_{21}=1$) is 175 GHz, which coincides exactly with the extrapolated f_T from modeled s-parameters. From the equivalent circuit, an intrinsic f_T ($f_T=g_m/(2\pi(C_{gs}+C_{gd}))$) of 286 GHz was calculated. The extrapolated f_{max} (MAG=1) from modeled s-parameters is 207 GHz. At higher frequencies (above W-band) a distributed model may become necessary.

B. Low-noise cryogenic HEMT amplifiers

Since silicon dopants in InGaAs possess a very low ionization energy, high carrier densities may be achieved also at cryogenic temperatures. As a result, InP HEMT allow for the design of extremely low-noise amplifiers operating at cryogenic conditions. Moreover, high performance can be achieved at relatively low V_{DS} because of the high mobility and carrier velocity in the InGaAs channel, meaning a very low dc-power dissipation of the amplifier. The combination of low noise and low power at cryogenic temperatures makes InP HEMT particularly attractive for certain space applications.

Figure 3 shows an InP HEMT-based cryogenic amplifier designed for 4-8 GHz [7]. The InP HEMT has four 50 μm wide gate fingers with a nominal gate-length of 0.12 μm and a ground-signal-ground (GSG) configuration with a pad pitch of 125 μm . In Fig. 4, the gain and noise performance at 15 K are presented showing the outstanding performance of the InP technology. The power consumption of this InP HEMT was only 3.7 mW.

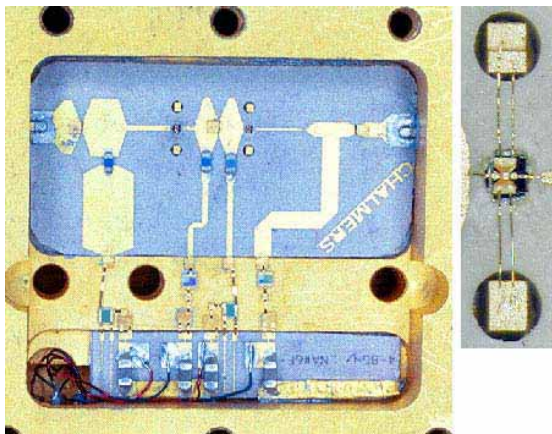


Fig. 3. Photograph of the cryogenic LNA and magnified detail of a InP HEMT including inductive feedback bonding wires for matching.

C. Heterostructure barrier varactors

The HBV is a symmetric varactor consisting of a high band gap semiconductor (barrier), surrounded by moderately doped modulation layers of a semiconductor

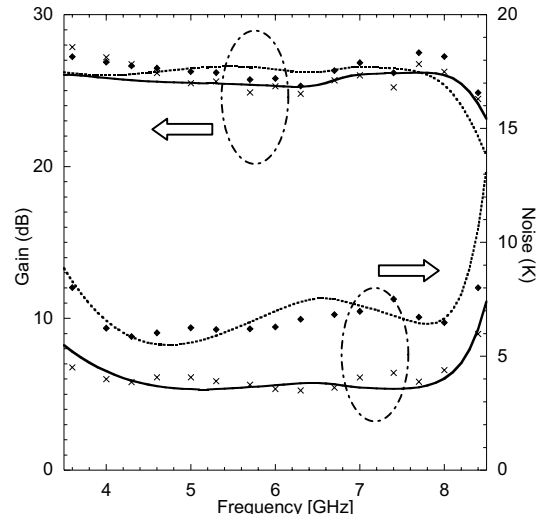


Fig. 4. Simulated and measured gain and noise temperature of the InP-based cryogenic LNA amplifier operating at 15 K (solid line and crosses, respectively). A commercial GaAs PHEMT device is included as a reference amplifier (dotted line and diamonds for simulations and measurements, respectively).

with a lower band gap. The barrier prevents electron transport through the structure. When an external signal is applied to the HBV, electrons are accumulated at one side and depleted at the other side of the barrier, causing a symmetric, voltage dependent capacitance. The main advantage with HBVs is the possibility to tailor the layer structure of the device for various applications. The power handling capability can be increased by stacking several epitaxial barriers. Furthermore, high order multipliers are easier to design due to the symmetry. The HBV generates only odd harmonics and require no bias.

At Chalmers, HBV research for THz transmitter generation has a long tradition [8]. In Fig. 5, a SEM micrograph shows a fabricated HBV with a new back-to-back geometry [9]. The planar HBV design incorporates a shorter finger with a larger cross section area, mainly to reduce the thermal resistance of the diode.

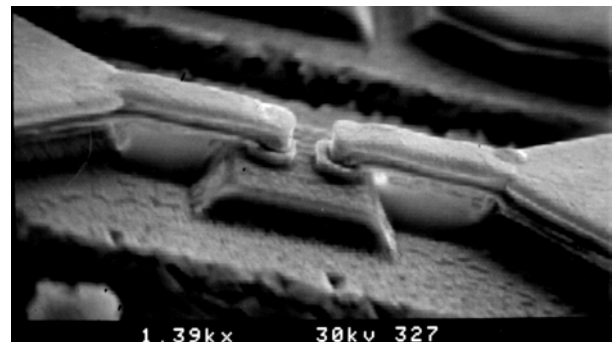


Fig. 5. SEM picture of an HBV diode with a planar design.

We have demonstrated that InP-based HBV diodes can be fabricated on a copper substrate without degrading the electrical characteristics [10]. As a result, the heat sink is improved and the spreading resistance (part of the

series resistance, R_s) is decreased. In a frequency tripler experiment demonstrated in Fig. 6, a maximum output power of 7.1 mW (8.5 dBm) was generated at 221 GHz with a maximum flange-to-flange efficiency of 7.9 %. The measured efficiency increases with the input power up to at least 90 mW, demonstrating that the heat sink is improved compared to earlier HBV experiments.

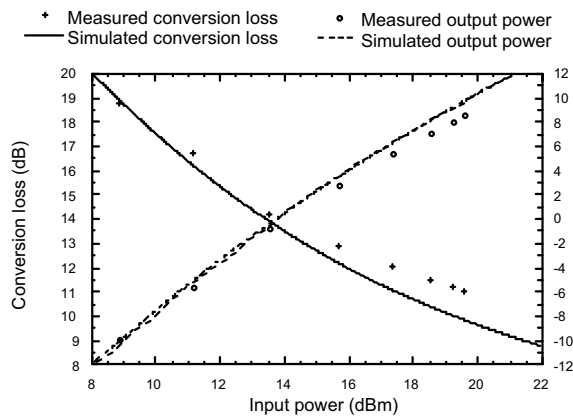


Fig. 6. Measured and simulated tripler conversion efficiency versus available power for the InP HBV tripler at a fundamental frequency of 74 GHz. A maximum output power of 7.1 mW was generated with an flange-to-flange efficiency of 7.9 % (11.0-dB conversion loss).

III. CIRCUIT DEMONSTRATORS

We have developed an in-house InP-based MMIC process. The process includes the HEMT, via-holes, mesa-resistors, and microstrip transmission line components.

Several different circuits have been designed in this process using equivalent HEMT models extracted from s-parameters measured up to 50 or 62 GHz. The models have later been validated by s-parameter measurements up to 115 GHz [11].

An F-band resistive mixer was designed, fabricated and characterized [12], see photo of circuit in Fig. 7. The LO-signal is applied to the left and matched to the gate of the device through an impedance transformer. Bias is applied from the top of the circuit through a radial stub filter. The sources of the device are grounded with via-holes. The RF-signal is connected from the right and a finger coupler serves as a combined DC-block and high-pass filter. The IF is extracted from the drain through a radial stub filter to the IF-output port, and a 5 k Ω mesa resistor sets the drain potential to 0 V. The mixer was simulated and optimized by using a harmonic balance simulator (MDS from HP) with the device model used in [13]. The device width was optimized (50 μ m gate width) to give low reflection loss at the RF-port without any output matching circuit. The simulated isolation between the LO-port and the RF-port is 12 dB at the gate voltage for minimum conversion loss.

The mixer was measured on-wafer using coplanar W-band probes for the RF and LO ports, and a coplanar V-band probe for the IF port. The LO frequency is 110 GHz and the RF is 112.5 GHz. A minimum conversion loss of

9 dB was measured with a saturated LO power of 4 dBm and an RF power of -14 dBm. The measured conversion loss versus LO power is plotted in Fig. 8.

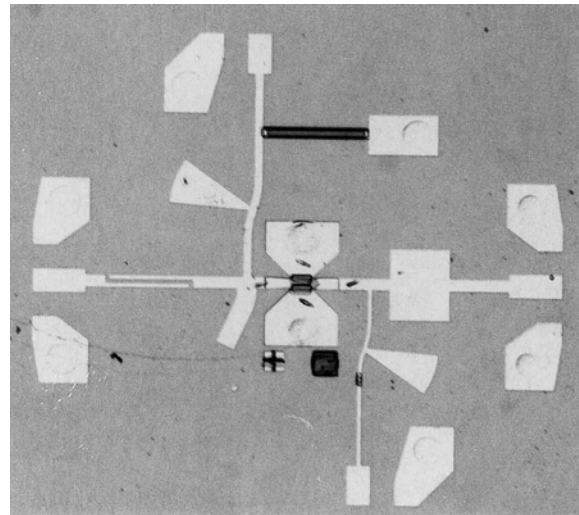


Fig. 7. Photograph of the F-band resistive mixer.

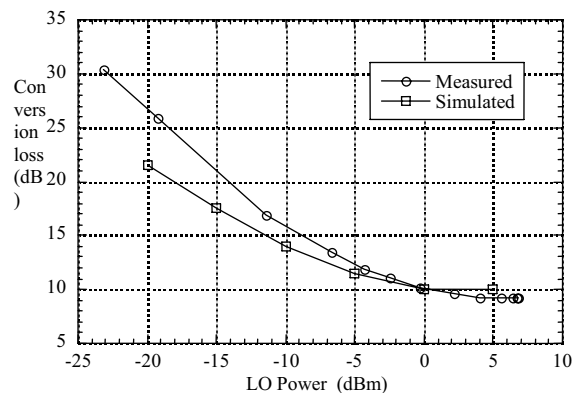


Fig. 8. Conversion loss vs. LO power (measured (circles) and simulated (squares)).

The gate-voltage for minimum conversion loss coincides well with simulations at LO-powers larger than -10 dBm. The measured and simulated optimum gate voltage (for minimum conversion loss) coincides within 0.05 V. At the optimum gate voltage, an LO power of 4 dBm is sufficient to saturate the mixer. The LO-RF isolation was measured to be 11 dB. Due to the lack of RF-power, we were unable to observe the 1 dB compression point, even at very low LO power levels.

Several 119 GHz InP HEMT amplifiers were also designed as a feasibility study within the Swedish satellite Odin receiver project [14]. Both one- and two-stage amplifiers were designed. A one stage amplifier was characterized on wafer with a W-band (75-115 GHz) network analyzer. A gain of 6 dB at 115 GHz was achieved. Another one-stage amplifier was inserted in a box with waveguide to microstrip transitions for the input and output signals. The waveguide probes were fabricated on alumina and the amplifier MMIC was

ribbon bonded and soldered to the circuit. A flange-to flange amplification of 3 dB was measured at 119 GHz at 77 K.

The MMIC process has now been developed to include thin film resistors, metal-insulator-metal capacitors, and spiral inductors with the down-scaled HEMT as the active device (50 nm gate length). We have designed extremely broadband resistive feed-back amplifiers and 94 GHz narrow-band amplifiers, see Figs. 9 and 10, to demonstrate and benchmark this process. The amplifiers will be characterized on wafer using a W-band VNA.

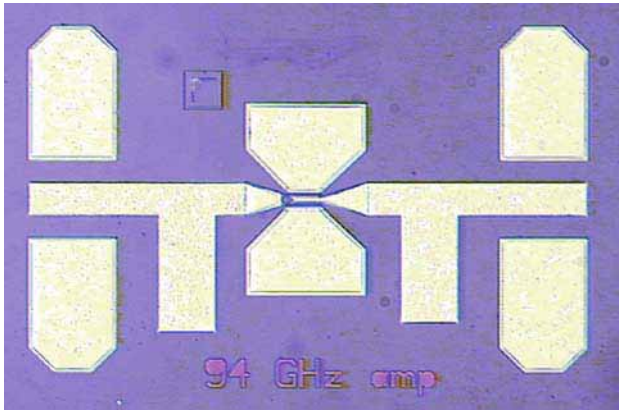


Fig. 9. Single-stage 94 GHz amplifier in the upgraded Chalmers InP MMIC process

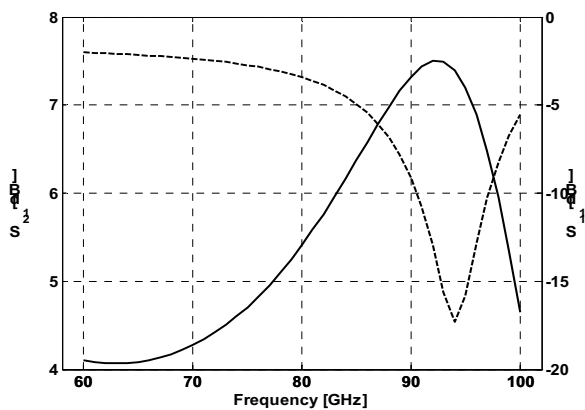


Fig. 10. Simulated S11 and S21 for the single-stage 94 GHz amplifier.

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