Future Trends in Si Technology/ICs for RF Applications

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***Abstract* — The continuous progress in semiconductor and module technology has indubitably fueled in the past years, together with the system design and algorithms, the telecommunication and wireless evolution characterized by a growing demand of new services and functions, the continuous decrease of mobile terminal costs, longer battery duration. The paper gives a brief description on the state of art and on going developments of key submicron RF Silicon technologies employed within the Wireless equipment, mainly taking into account the 2.5-3G cellular-phone and emerging WLAN applications as the natural interconnection of wireless communications with Internet. While high density CMOS evolution still represents the core technology development also for RF dedicated Silicon, Silicon-Germanium or Silicon Germanium Carbon processes, differentiating factors both in term of overall performances and costs rely now also on availability of integrated good quality passives, RF MEMS as well as RF modules and cost effective packaging technology.**

I. INTRODUCTION

Wireless Technology offers new services, freedom, and potential "anytime, anyplace" communications. Consumers are always answering very enthusiastically to new service proposals as soon as availability, cost and quality of those services are in line with the perceived advantages deriving from their use.

The key challenges of this growth, which cannot be halted, reside on the ability of equipment manufactures of keeping pace with the users' expectations on weight/volume, use friendless, battery duration constrains of mobile terminals despite growing performances, insuring the necessary reliability, and cost effectiveness.

II. WIRELESS MARKET TECHNOLOGIES NEEDS

After the voice communication boom that has characterized telecommunications and specially the mobile cellular spectacular growth of the end of the century, most analysts interpret the current market indicators as the first sign of a recovery that could last for several years, where the 2003 can be the first year of the mobile data transmission era.

The 3rd and 4th multi mode, multi band wireless terminal generation promising ubiquous data (Internet, Multimedia) and video services let additionally forecast a wider pervasion of the mobile multi-functions terminals, access points, combined optical-wireless ground network equipment connections.

In the last year two additional factors characterized this market segment yielding in a renewed push for better and cheaper solutions. First of all handset makers, as well as new comers from networking, beside the continuous investments on the newest applications development, mechanical case design, users' interface SW, they are progressively focusing their resources on higher levels of supply chain (production logistics and subcontracting, distribution, branding…). In addition, due to the progressive move towards a pure Consumer Market of the mobile terminals, chip suppliers are in the meantime asked to provide at least for large volume applications a complete integrated solution in term of RF modules, to minimize the upper level integration effort.

Progress in semiconductors technologies, processing algorithms, system design, displays, batteries, substrate modules and packaging techniques have then to provide suitable solutions for the new requirements. While high level integration and System on Chip approaches (SOC) have given a satisfactory solutions for a large digital functions integration, multi band multimode RF module can now provide an effective way of reducing the large number of discrete or partially integrated components still required by the RF section of the mobile terminal. Micro modules assembly technology and System on Package (SOP) in mobile handset will progressively have a growing impact on the size miniaturization and the overall supply reduction requirements.

III. CMOS/BICMOS TECHNOLOGY EVOLUTION

The continuous improvement of CMOS technologies plays a fundamental role as core processes for most of sub-micron dedicated families (fig. 1/2). Today's 90nm minimum feature size technology guarantees a logic complexity up to 360K gate/mm^2. The continuous dimension shrinkage, together with the development of Cu low resistivity interconnects and low K dielectric, is giving to pure CMOS ICs renewed capability that will yield on a higher operative frequency and computational power to comply with the 3G and 4G request. Moore's law, applied to gates and memory density, will remain valid for the next 7 to 10 years.

Nevertheless, a few signs of Moore's law saturation is visible due to:

1- the necessity to introduce more and more complex material, e.g. high K gate oxide /metal gate to insure producibility;
2 - thermal issues due to standby power;
3 - the complexity and cost of new designs;

4 - the financial effort to allow processes evolution.

CMOS itself can do a lot to improve the RF performance, e.g. in term of Ft or Fmax, even if at the expenses of reduced operating voltage, down to 1 Volt Vds or below.

High-speed technologies, specifically developed for RF and low power consumption application, directly derive from CMOS core processes with addition of a few specific steps to introduce heterojunction Bjt transistors. Bipolar transistors with silicon/silicon-germanium base and even carbon doped silicon-germanium epitaxial base to reduce base width down to 30nm (fig 3) are currently available. On the SiGe:C BiCMOS 0.13 um technology compatible with 0.13um CMOS generation an impressive 150 GHz Ft and Fmax in excess of 120 GHz has been measured at 1.5V Vce. This type of technologies will provide optimum NF lower than 1dB at frequency up to 6 GHz making this a very competitive choice for highly integrate WLAN solutions.

This is achieved once again at expenses of a substantial reduction of C-E breakdown voltage; in case higher voltage transistors, e.g. with up to 5 V Lvceo, are necessary, this can be achieved with additional process steps and reduced Ft.

III. PASSIVE DEVICES/MEMS/MODULES

Together with the use of the state of art silicon technology for higher computation power, the reduction of ICs and passive components count has been a success key issue of the mobile phone evolution to continuously get lower total cost per function over the years. One way to save external passives, a need particular evident on RF stages, is to avoid them by using suitable Architecture/Circuit topology. Homodyne solution, image rejection filters as well as SC and gmC filters are just a few examples of it. Process production spreads can now be controlled by the use of on chip automatic tuner technique or wafer level trimming during the final testing phase. There is nevertheless a variety of reasons why this cannot be realized without having an internal passive device of good quality to achieve the required performances jointly with low power consumption.

CMOS/BICMOS process road map for RF integrated solutions takes into account inductors, capacitors, varactors and resistors passive performance requirements. Their availability often introduces the same cost penalty, due to additional process steps and higher substrate cost. E.g. high quality inductors require thick interconnect metal layers (Cu) and high resistivity substrate (>10ohm*cm) to limit magnetic losses. Metal insulator metal structures of high specific capacitance require Tox of few tens on nm (30-50) and specific high permittivity insulator materials yielding once again in a higher process cost. If RF designer embraces a larger environment including micro-module or System on a Package (SOP) solutions (fig. 4), his toolbox will enrich of new possible devices and possibility to merge technologies for a best overall performance. This is the case of MEMS/based integrated RF module architecture (fig. 5). On the top of low cost and good RF substrate like resistivity silicon of glass (Integrated Passive Device substrate – IPAD), passive components (high precision resistor, high Q inductor/capacitor) are realized with standard semiconductor process technique, which does not require any micro-machines steps. The active circuitry will be bumped on the top of this substrate together with necessary micro-capped MEMS based components (Varcap, BAW).

RF micro-systems technology will provide innovative path for size and cost reduction by increasing the level of integration and by offering the possibility of new, multi-band multimode radio architectures (fig. 6). Further evolution into subsystem modules integrating physical layer interface and protocol Stack will make faster and cheaper the high level integration performed by the mobile terminal manufacturer.

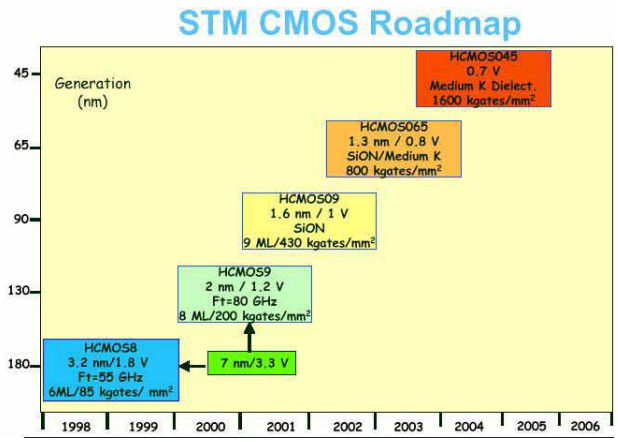

Fig.1 - CMOS Road Map

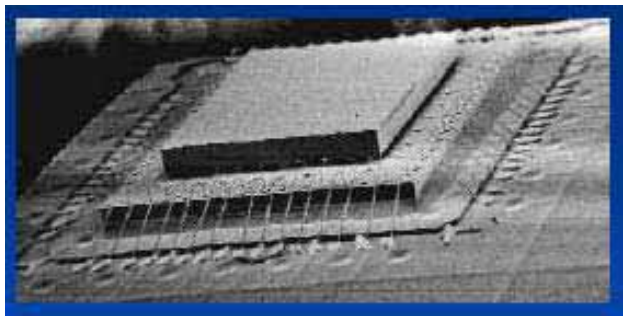

Fig 4 - Silicon on Silicon chip Assembly (RF FlipChip)

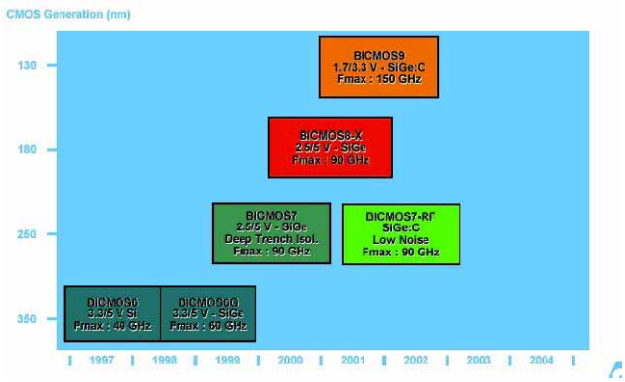

Fig.2 - BICMOS Road Map

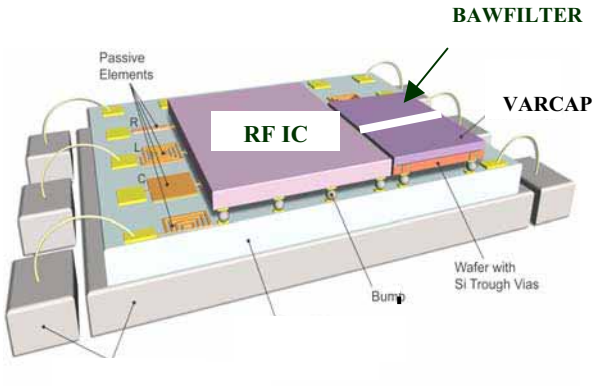

Fig.5 - RF Module on Glass Substrate (IPAD)

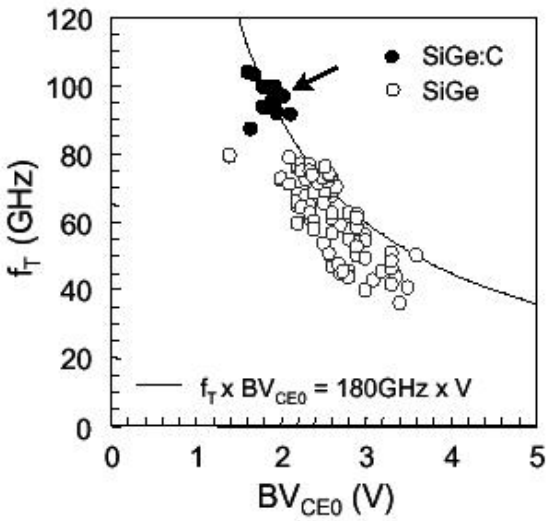

Fig.3 - Ft for 0.25 um BiCMOS Si-Ge: C

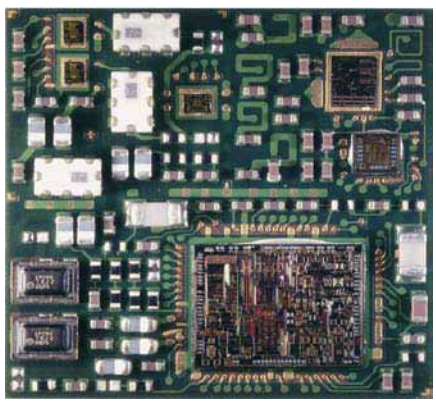

Fig.6 - Single package GSM Radio Module on Glass Substrate