

C-band 10-Watt HBT High-power Amplifier with 50% PAE

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ABSTRACT

The design and measurement of a C-band HBT high-power amplifier (HPA) is discussed. The amplifier is realised in the HB20P power HBT process of UMS. The HPA combines a high average output power of 9 Watt with both a high gain of 21.6 dB and a high power added efficiency (PAE) of 50% over about 20% bandwidth at the nominal 8 V collector voltage. At a collector voltage of 10 V an average output power of 10.3 Watt has been measured. The high PAE is realised with the help of an inverse class F harmonic termination scheme. A good agreement between measurement and simulation results is demonstrated.

INTRODUCTION

The design and measurement results of a high-power amplifier intended for radar applications are discussed. The design is realised with the help of the HB20P power heterojunction bipolar transistor (HBT) process of UMS. The use of this HBT process offers the combination of a high power density (> 3 W/mm) with high-gain and the ability to have a single bias supply. Until recently the use of HBT technology for the realisation of high-power amplifiers was not wide-spread due to the low reliability. This issue is resolved for the HB20P process of UMS. For this process the Mean Time To Failure is exceeding 10^6 hours at a junction temperature of 125 °C [1]. The integrated emitter ballast resistors and the thick thermal drain on top of the transistor guarantee the thermal stability [2] of the transistor.

In the remainder of this paper the amplifier design and the measurement results of a number of power amplifiers from two different wafers will be discussed.

AMPLIFIER DESIGN

The design focussed at the development of a C-band high-power amplifier that has an output power of 10 Watt, a PAE of at least 45% and a gain of at least 20 dB. To realise the required output power, 16 transistors are used in parallel in the output stage. Each transistor has 8 fingers with a width of 2 μ m and a length of 30 μ m. The load impedance used in the design is based on load-pull measurements. To obtain the highest possible PAE an inverse class F [3] matching scheme is used. In this high-power amplifier, an open is presented at the output of the transistors at the second harmonic frequency. Both the output power and power added efficiency will increase through the utilisation of the mentioned inverse class F matching scheme, as can be concluded from the results depicted in figure 1. The power added efficiency increases from 50.5 % to 64.7% and the output power increases at the maximum power added efficiency point from 28.7 dBm to 29.2 dBm.

The electrical stability of the transistors is enhanced via the application of a parallel RC network at the input of each transistor, see figure 2. The used resistor has a value of 30 Ω and the capacitor has a value of 3 pF. The K-factor depicted in figure 3 demonstrates that without the stabilisation network the transistor is only unconditional stable above 5.8 GHz. When the stabilisation network is applied the transistor is unconditional stable for frequencies above 0.4 GHz. Below this frequency off-chip decoupling capacitors have to be applied to stabilise the amplifier. In addition, not only the sensitivity to load impedances presented at the input and the output of the transistors outside the frequency band is reduced with the application of the series RC stabilisation network but also the occurrence of parametric oscillations is prevented [4].

The high-power amplifier consists of two stages with 4 transistors in parallel in the first stage and 16 transistors in the second stage. Special attention has been paid to the design of the interstage matching network. A fourth order matching network is used to ensure that over the entire frequency band both at the load and source side of the network a matching of better than 20 dB is achieved. In addition, electromagnetic field simulations have been used to optimise the performance of all matching networks.

The stability of the entire high-power amplifier is checked with the help of the method described in [5]. No oscillations were detected in this way.

MEASUREMENT RESULTS

The realised amplifier is depicted in figure 4. In figures 5-7, a comparison is shown between the simulated and the measured small-signal performance. The results show a very good agreement between both results. This agreement shows both the validity of the used models and the used design approach. The measured large-signal performance at the nominal collector voltage of 8 V is shown in figures 8 and 9. Measurement results of three typical power amplifiers from two different wafers are shown. An average output power of 9 Watt, a gain of 21.6 dB and a PAE of 50% is measured over the 5-6 GHz frequency band. The output power variation between the amplifiers is less than ± 0.5 dB over the before mentioned frequency band. Within this frequency band a peak output power of 10 Watt and a peak PAE of 54% is measured. Thanks to the high breakdown voltage of the HB20P process it is also possible to use the amplifiers at higher collector voltages. In figure 10 a comparison of the measured output power for different collector voltages is shown. The results show a measured average output power of 10.3 Watt and a peak output power of 11.7 Watt at a collector voltage of 10V.

CONCLUSIONS

The design and measurement results of a C-band high-power amplifier are discussed. At the nominal collector voltage of 8 V the measured average performance is excellent and very close to the design goals. These results were obtained in a single design iteration. At a collector voltage of 10 V a maximum output power of 11.7 Watt is measured with a gain of more than 20 dB. An excellent average power added efficiency of 50% is realised over the 5-6 GHz frequency band. This high power added efficiency has been obtained due to the application of an inverse class F harmonic termination scheme.

ACKNOWLEDGEMENT

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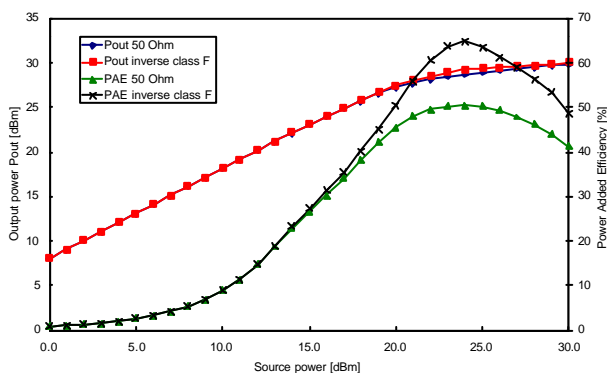


Figure 1: Simulated output power and PAE of an $8 \times 30 \mu\text{m}^2$ HBT at $f=5.5$ GHz and $V_c = 8$ V.

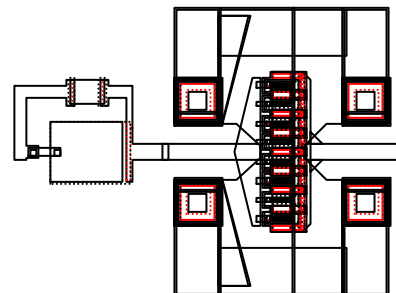


Figure 2: RC stabilisation network and unit transistor cell.

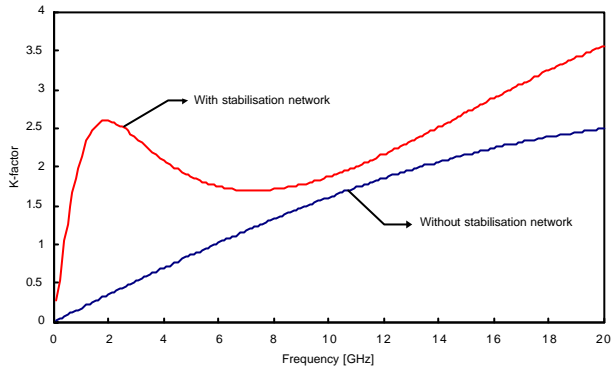


Figure 3: Stability unit transistor cell with and without stabilisation network (see figure 2).

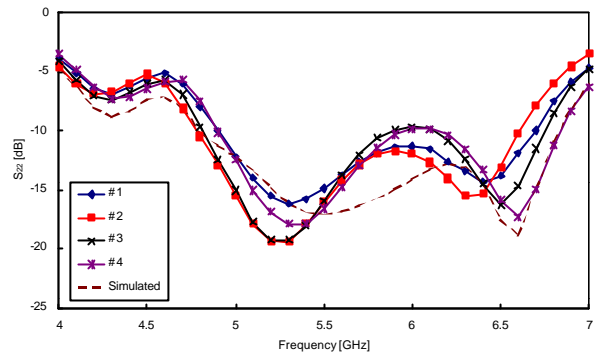


Figure 7: Comparison measured and simulated S_{22} .

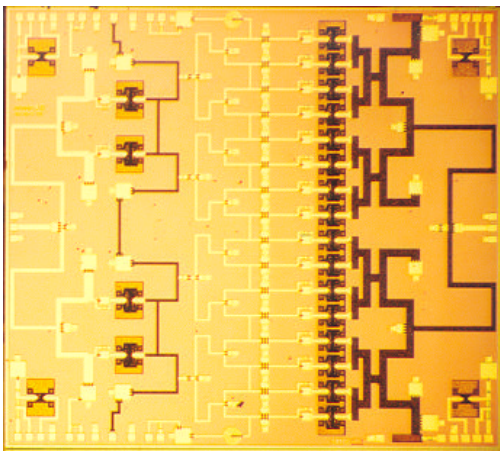


Figure 4: Photograph 10-Watt HPA ($6.45 \times 5.79 \text{ mm}^2$).

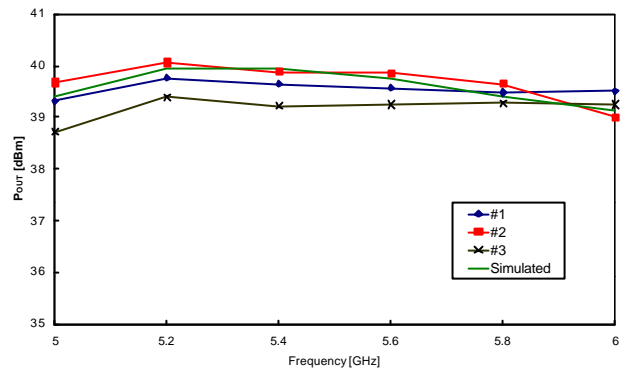


Figure 8: Measured output power at $V_C=8 \text{ V}$ and $P_S=18 \text{ dBm}$.

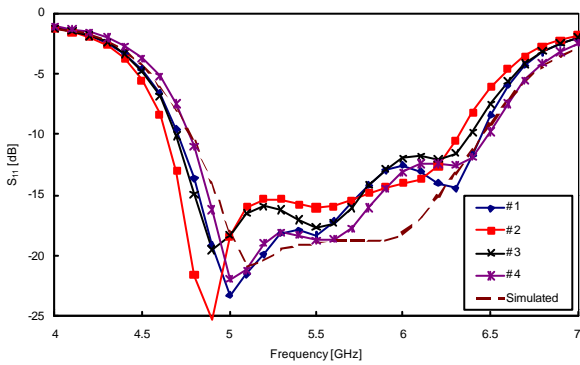


Figure 5: Comparison measured and simulated S_{11} .

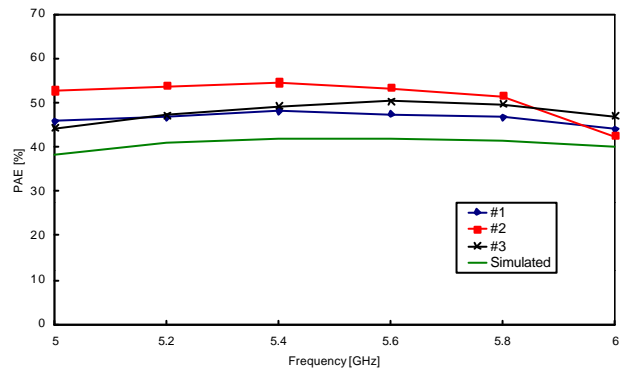


Figure 9: Measured PAE at $V_C=8 \text{ V}$ and $P_S=18 \text{ dBm}$.

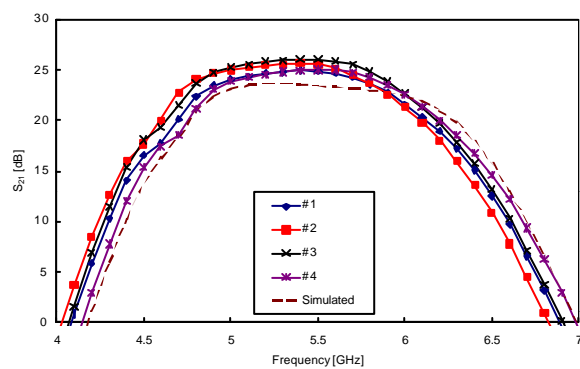


Figure 6: Comparison measured and simulated S_{21} .

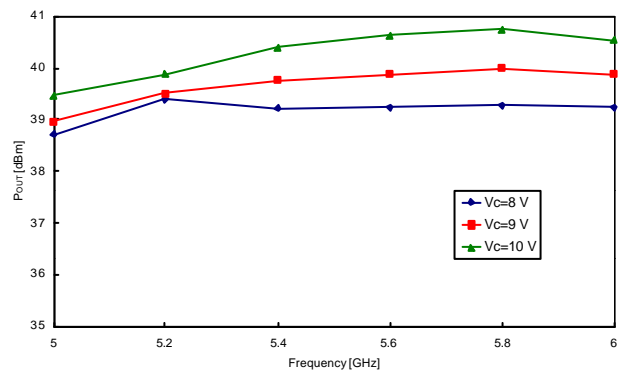


Figure 10: Measured output power as function of the collector voltage at $P_S = 18 \text{ dBm}$