A 4-bit 7.5 GHz A/D Converter

Petros Tsenes, Nikolaos Uzunoglu

National Technical University of Athens
School of Electrical and Computer Engineering
9 Heroon Polytechneiou Str., 157 73 Zografou, Athens, Greece, tel:++30 210 7722289

***Abstract* — Based on a conventional flash architecture a 4-bit GaAs analog to digital (A/D) converter has been designed using OMMIC-Philips GaAs foundry and particularly its commercial enhancement/depletion mode 0.18 µm pHEMT technology process. The ADC operates at 7.5 GHz sampling rate with full power analog input bandwidth from DC to Nyquist frequency. Differential source coupled FET logic (SCFL) was used and the complexity of the whole chip is more than 1900 active devices. The converter can be used in radar and software radio applications where there is requirement for high sampling rates in order the superheterodyne architecture for the down conversion to be avoided.**

I. Introduction

Analog to digital converters are ubiquitous, critical components of signal processing systems, which operate on a wide variety of continuous time signals such as medical imaging, radar, instrumentation, consumer electronics and telecommunications. Characteristics of the ADCs play a key role in the performance of these systems, which convert the continuous time signals to discrete time, binary coded form. Because of the large number of signal types, there is a great variety of different types of ADCs, each one having different resolution and sampling rate. The highest sampling rate attained so far is a few Gsamples/s [1], something that is related to the ability of the comparator to transition from sample to hold mode and/or to transition from hold to sample mode. This can be directly related to the performance of the device technology used to fabricate the ADC, in terms of the unity-current-gain frequency, f_T, and/or device parasitics.

Among the different architectures that have been developed, flash (parallel) architecture provides the fastest ADCs. The parallelism of this type has a significant drawback when high resolution conversion is desired, namely the number of comparators grows exponentially with the number of the bits. That is why flash ADCs are the best solution for measurement equipment and radar applications where very high sampling rate (above 1 GS/s) and quite low resolution (4-8 bits) can be very useful.

Although ADCs using Si and having sampling rates above 1 GS/s have been published [2]-[3], the fastest ADCs are fabricated using GaAs. Some approaches use HBT technology [4]-[5], which has the advantage of very good V_{BE} matching among the bipolar transistors and as a result they provide good linearity for an ADC. On the other hand, circuits that are fabricated using MESFET and HEMT GaAs technology [6]-[9] have the advantage of a very small gate leakage which means that the droop in the held voltage in the track and hold circuits is much slower.

II. Architecture of the Converter

The ADC is a 4-bit flash converter using binary encoding. A schematic of the ADC architecture is shown in Fig. 1. The flash approach that was chosen in order the speed of the quantizer to be maximized, requires sixteen comparators for 4-bit resolution and the overflow bit. The converter is also consisted of master-slave latches, encoding logic, output latches, output drivers and clock distribution circuitry.

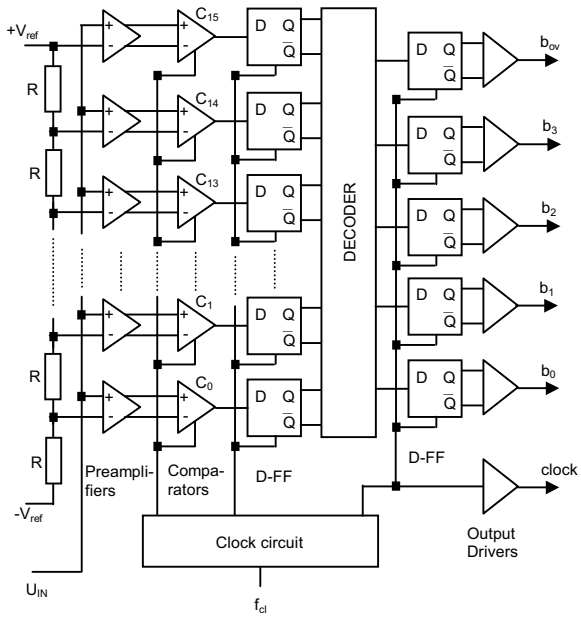

Fig. 1. Schematic of the 4-bit converter.

To achieve high speed and good noise margin differential source-coupled FET logic with passive loads was used. To minimize clock feedthrough to the analog input and reference ladder a preamplifier precedes each of the clocked comparators. It is consisted of an input buffer, a differential stage and an output buffer. Using source follower buffers at the analog and reference inputs, a very linear capacitance is achieved. Moreover, the additional amplification decreases the response time of the comparator and the probability of metastable states. The clocked comparator is a SCFL latch with cascode stages that are decreasing the response time. The circuit diagram of the preamplifier and the comparator is shown in Fig. 2.

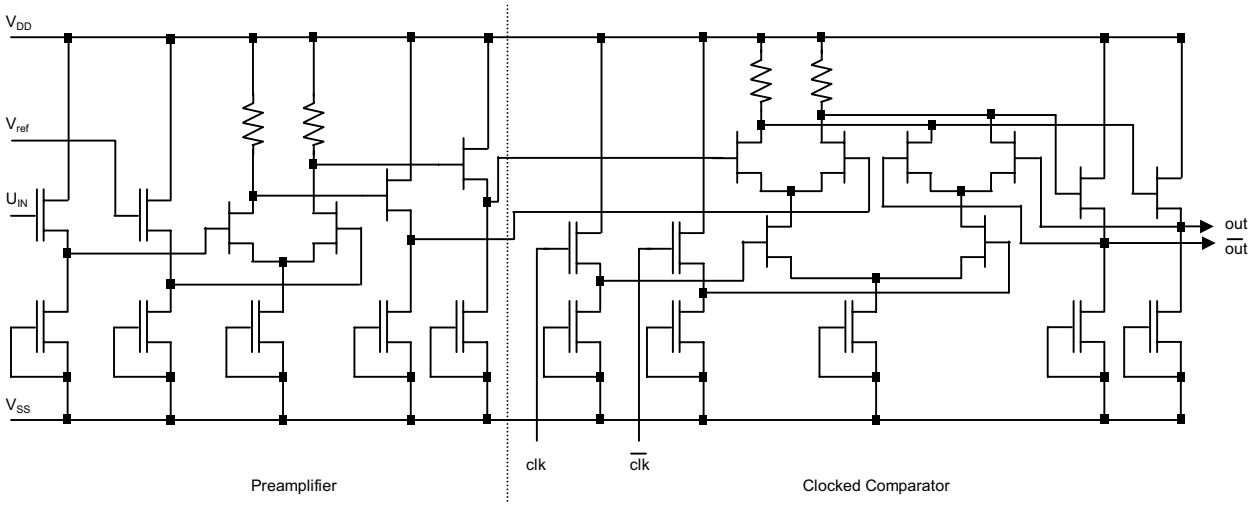

Fig. 2. Circuit diagram of the preamplifier and the comparator.

Master-slave latches, which latch the comparator's outputs, consist actually of two comparators that are cascaded together to increase the gain. They are also pipelined which means that when the first is sampling input data the second is amplifying the previous input data. They provide the comparator signals to the encoding logic, which is composed of SCFL NOR gates for the "thermometer to 1-of-n-code" translation. A wired OR circuit is being used in order the binary encoding to be achieved. This circuit is designed in such a way that it can provide the output latches with differential signal and as a result problems that may exist due to temperature and process variations are reduced. Actually, the wired OR circuit although it provides the "ones" and the "zeros" of the code and as a result has increased complexity compared to a conventional one, it occupies the same area on the chip. Finally, five output latches, one for each bit and one more for the overflow bit, are behind five 50 Ω output drivers.

III. Clock Circuit

The clock signal that is necessary for the clocked comparators and the master-slave latches is generated and distributed inside the chip from an internal clock circuit, which has as an input signal an external sine. The clock circuit contains, among other sub-circuits, two 2:1 frequency dividers and a multiplexer, which is controlled by external signals, and enables the clock signal that is necessary for the output latches to be chosen among three signals having different frequencies. So, although the comparators and the latches that follow them operate at f_{clock} frequency the output latches can operate at f_{clock}, $f_{clock}/2$, $f_{clock}/4$ according to the user's wish and the ability of the equipment that is used for the characterization of the circuit.

The block diagram of the clock circuit is shown in Fig. 3. Differential source-coupled FET logic with passive loads was used for the design of the clock circuit. A differential signal is generated from an input buffer, which operates as a differential amplifier having one of its inputs grounded. In detail the input buffer consists of source followers at the input and the outputs and two differential amplifiers providing sufficient gain in order the clock signal to reach the desirable voltage swing. After the input buffer the clock signal is provided to the cascaded 2:1 frequency dividers and as a result a clock signal having the double period and a clock signal having the fourfold period are also available. Each of the two 2:1 static frequency dividers consist of a master-slave D flip-flop with output fed back to the data input [10]. Source followers are employed between the latches to provide the necessary voltage level shifting.

The multiplexer operates as a triple switch giving us the opportunity to select the frequency (among three choices) at which the output latches operate. Delay buffers are also included at different places in the clock circuit in order the propagation delays through the frequency dividers and the multiplexer to be balanced. The appropriate placement of the delay buffers was also selected taking into account that the layout of the clock circuit has to be as compact as possible and that the clock signal must distributed at different points of the circuit having specific phase shift.

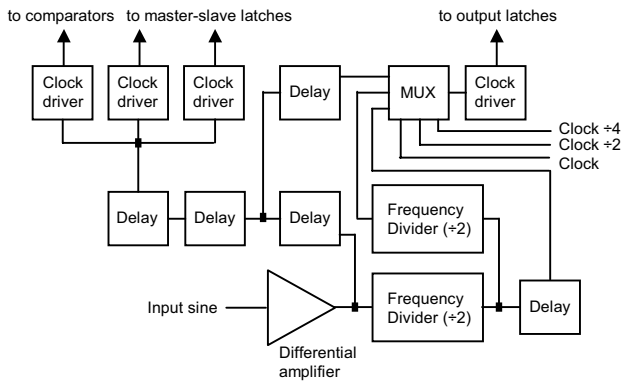

Fig. 3. Block diagram of the clock circuit.

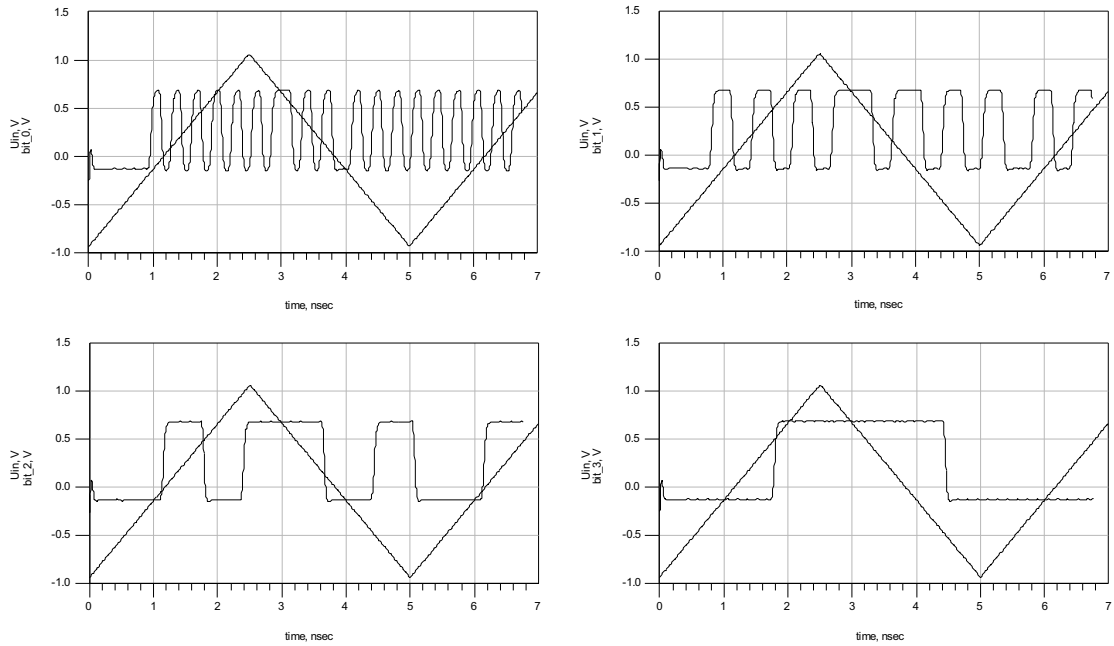

Fig. 4. 4-bit digital outputs for a full scale input ramp at 7 GS/s sampling rate.

Clock drivers provide finally the comparators and the master-slave latches with the necessary clock signal. Each of them consists of a differential pair and two cascaded source followers at the output. The source followers have been designed having successive increased gate width and as a result except their usage as level shifters they have good driving capability. It should also be mentioned that the clock lines that cross vertically the circuit are terminated with the appropriate resistance and capacitance. Finally, the clock driver of the output latches provides with the clock signal an output driver and consequently the clock is available to be displayed and used, if it is necessary, as a trigger signal for the measurement equipment.

IV. Results

The preamplifiers that precede the clocked comparators are designed in such a way that the full scale range is ±1V and therefore quantization step is 125 mV. In Fig. 4 simulation results of the 4-bit digital outputs for a full scale input ramp and 7 GS/s sampling rate can be seen. Due to the pipelining of the latches there is a delay of three clock cycles and it should be mentioned that the overflow bit is not shown. During the next months evaluation and characterization (static and dynamic) will be performed with on-wafer measurements [11].

The necessary external DC voltages for DC power supply are ±2.5 V, while for the creation of the reference voltages are ±1 V. The total power dissipation is approximately 5500 mW. In Fig. 5 the layout of the circuit can be seen.

V. Conclusion

In this paper the design of a 4-bit GaAs analog to digital (A/D) converter has been presented. The ADC was designed and will be fabricated using OMMIC-Philips GaAs foundry and particularly its commercial enhancement/depletion mode 0.18 μm pHEMT technology process. The ADC operates at 7.5 GHz sampling rate with full power analog input bandwidth from DC to Nyquist frequency. Differential source coupled FET logic (SCFL) was used and the complexity of the whole chip is approximately 1900 active devices.

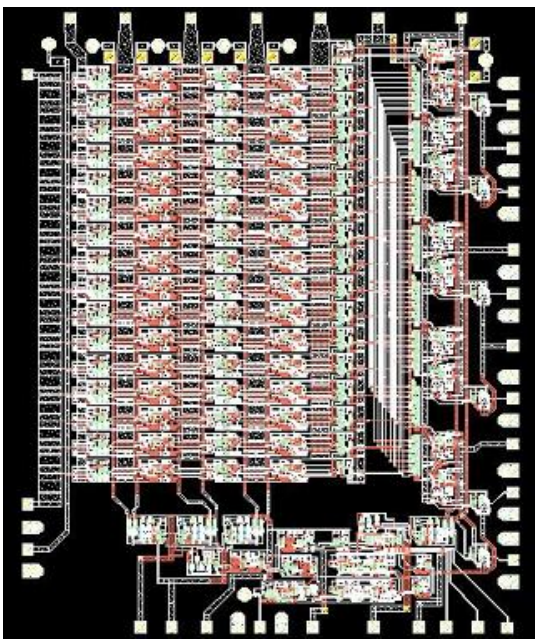

Fig. 5. Layout of the circuit.

Its sampling rate is one of the highest that have been reported and due to very careful design the measurements are expected to be as satisfactory as simulation results are. Finally, an attempt will be made two such ADCs to be cascaded in order higher resolution to be succeeded.

REFERENCES

[1] R. Walden, "Analog-to-Digital Converter Technology Comparison," in *Proceedings of the IEEE GaAs IC Symposium,*1994, pp. 217-219.

[2] T. Wakimoto, Y. Akazawa, and S. Konaka, "Si Bipolar 2 GS/s 6b Flash A/D Conversion LSI," in *Proceedings of the IEEE International Solid State Circuits Conference,*1988, pp. 232-233.

[3] K. Uyttenhove, A. Margues, and M. Steyaert, "A 6-bit 1 GHz Acquisition Speed CMOS Flash ADC with Digital Error Correction," in *Proceedings of the IEEE Custom Integrated Circuits Conference,2000*, pp. 249-252.

[4] K. Poulton, K. Knudsen, J. Corcoran, K. Wang, R. Nubling, R. Pierson, M. Chang, P. Asbeck, and R. Huang, "A 6-bit, 4GSa/s ADC Fabricated in a GaAs HBT Process," in *Proceedings of the IEEE GaAs IC Symposium,*1994, pp. 240-243.

[5] K. Nary, R. Nubling, S. Beccue, W. Colleran, J. Penney, and K. Wang, "An 8-bit, 2 Gigasample per second Analog to Digital Converter," in *Proceedings of the IEEE GaAs IC Symposium,*1995, pp. 303-306.

[6] T. Ducourant, M. Binet, J. Baelde, C. Rocher, and J. Gibereau, "3 GHz, 150 mW, 4 bit GaAs Analogue to Digital Converter," in *Proceedings of the IEEE GaAs IC Symposium,*1986, pp. 209-212

[7] T. Ducourant, D. Meignant, P. Bertsch, and M. Wright, "A 5 bit, 2.2 GS/s Monolithic A/D Converter with Gigahertz Bandwidth, and 6 bit A/D Converter System," in *Proceedings of the IEEE GaAs IC Symposium,*1989, pp. 337-340.

[8] R. Hagelauer, F. Oehler, G. Rohmer, J. Sauerer, and D. Seitzer, "A Gigasample/Second 5-b ADC with On-Chip Track and Hold Based on an Industrial 1-μm GaAs MESFET E/D Process," *IEEE Journal of Solid-State Circuits*, vol.27, no. 10, Oct. 1992, pp. 1313-1320.

[9] F.Oehler, J. Sauerer, R. Hagelauer, D. Seitzer, U. Nowotny, B. Raynor, and J. Schneider, "A 3.6 Gigasample/s 5 bit Analog to Digital Converter using 0.3 μm AlGaAs-HEMT Technology," in *Proceedings of the IEEE GaAs IC Symposium,*1993, pp. 163-166.

[10] Z. Lao, W. Bronner, A. Thiede, M. Schlechtweg, A. Huelsmann, M. Rieger-Motzer, G. Kaufel, B. Raynor, and M. Sedler, "35-GHz Static and 48-GHz Dynamic Frequency Divider IC's Using 0.2-μm AlGaAs/GaAs – HEMT's," *IEEE Journal of Solid-State Circuits*, vol.32, no. 10, Oct. 1997, pp. 1556-1562.

[11] IEEE Standard for Digitizing Waveform Recorders, Std 1057-1994.