CMOS and SiGe Bipolar Circuits for High-Speed Applications

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***Abstract*— Recently, CMOS has been demonstrated to be a viable technology for very-high-bit-rate broadband and wireless communication systems up to 40 Gb/s and 50 GHz. Advances in device scaling and doping-profile optimization have also resulted in SiGe bipolar transistors with impressive performance, including cut-off frequencies of more than 200 GHz. This paper presents advances in circuit design which fully exploit the high-speed potential of a 0.13 μm CMOS technology up to 50 GHz and of a high-performance SiGe bipolar technology up to 110 GHz operating frequency. The combination of advanced circuit techniques and a state-of-the-art fabrication-process technology results in continuing the upward shift of the frequency limits.**

I. Introduction

Ubiquitous access to information, anywhere, anyplace, and anytime, will require whole new kinds of information systems. This demand for novel communication systems will translate into innovation in emerging technologies, circuit-design methodologies and fabrication techniques. At the core of these approaches, heavy emphasis is placed on finding the right match between circuit techniques and fabrication-process technology. The current cycle sees radio frequency (RF) and monolithic microwave integrated circuit (MMIC) engineering having grown rapidly in importance in recent years, stimulated in particular by booming digital communications. For many years IC's for high-speed communications were dominated by very fast, specialized GaAs and InP processes [1], [2], [3]. Their high cut-off frequencies and high breakdown voltages present a unique combination which addresses some major issues. The highest operating frequencies reported so far for frequency divider circuits both in SiGe and III-V technologies are in the range of 70 GHz to 100 GHz [4], [5], [6], [7], [8], [9]. Recently, high-speed CMOS IC's have been presented for very high throughput rates [10], [11], [12], [13], [14]. CMOS solutions are very economical because of the lower production costs, higher yield and integration density that can be achieved.

In this paper we present recent advances in circuit design which fully exploit the high-speed potential of CMOS and SiGe process technologies up to 110 GHz operating frequency. Key circuits for communications systems, such as frequency dividers, multiplexers (MUX) and demultiplexers (DEMUX) and voltage-controlled oscillators (VCO) are presented in a 0.13 μm standard CMOS technology [15] and in an advanced SiGe bipolar process based on the technology presented in [7]. It uses a double-polysilicon self-aligned emitter-base configuration with effective emitter width of 0.15 μm. The SiGe:C base is grown by selective epitaxy. The maximum transit frequency f_T of the transistors is 200 GHz [16].

II. A 27 GHz CMOS Static 2:1 Frequency Divider

High speed static frequency divider circuits are important functional blocks in a variety of applications, ranging from wireless communications to broadband optical fiber communication systems. Fig. 1 shows the block diagram of the 2:1

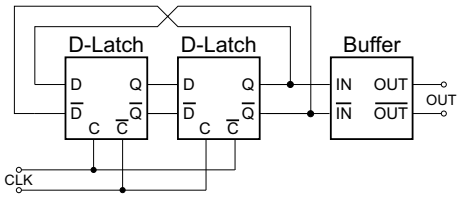


Fig. 1. Block-diagram of a 27 GHz static frequency divider [17].

static frequency divider [17]. The internal dividing function is based on a master-slave D-type flip-flop by connecting the inverted slave outputs to the master inputs. A separate buffer decouples the divider core from the 50 Ω output load. Fig. 2

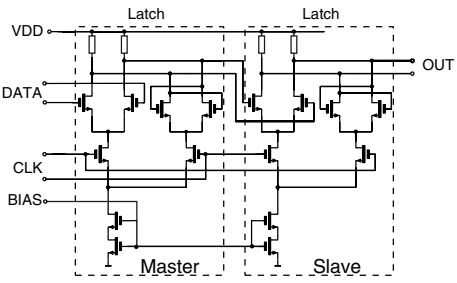
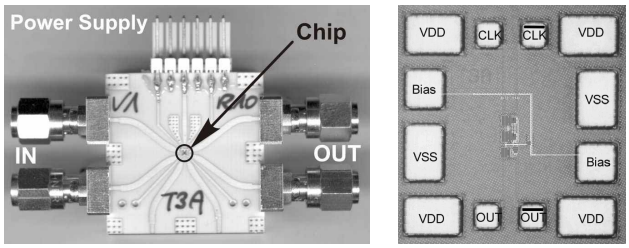


Fig. 2. Schematic diagram of the master slave flip-flop [17].

shows the schematic diagram of the master slave flip-flop MS-FF used in the divider, the MUX and the DEMUX circuit. This type of logic is based on current sources and differential amplifiers acting as current switch. In combination with the use of differential signals this allows operation with a reduced voltage swing in the range of 0.3 Vpp to 0.5 Vpp. This low voltage swing is essential for achieving high operating speed and low power consumption. To evaluate the performance of the divider IC, the chip was mounted on a 30 x 30 mm^2 0.51 mm RO4003 microwave substrate with SMA connectors

for differential input and output signals. Fig. 3(a) shows the high frequency test fixture and Fig. 3(b) the chip photo of the divider IC.



(a) size: 30 x 30 mm^2 (b) size: 0.47 x 0.49 mm^2

Fig. 3. 27 GHz divider test fixture and chip photograph [17].

Fig. 4 shows the input sensitivity versus input frequency. The circuit shows broadband performance up to operation frequencies of 24 GHz with input levels less than 0 dBm. The maximum operating frequency is 27 GHz. The divider core draws 20 mA and the output buffer 10 mA from a single 1.5 V supply. With this supply voltage, the divider consumes 45 mW. The divider features high input sensitivity and a 50 Ω output buffer.

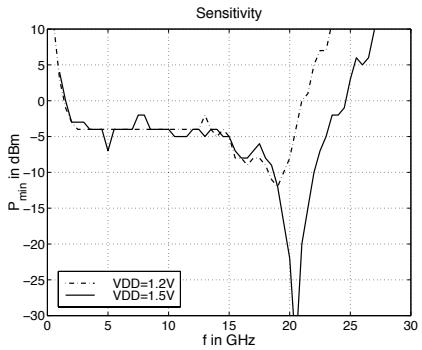
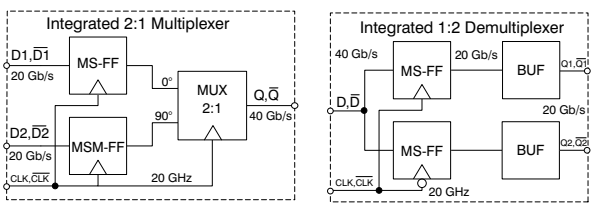


Fig. 4. Input sensitivity of the 27 GHz static divider [17].

III. A 40 Gb/s CMOS 2:1 MUX and 1:2 DEMUX

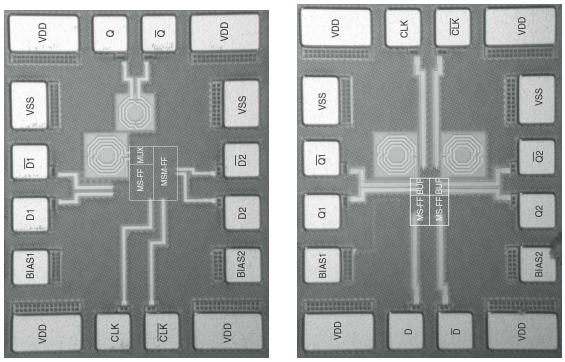
Fully integrated 2:1 MUX and 1:2 DEMUX ICs in CMOS operate up to 40 Gb/s data rate [18]. The MUX uses inductive peaking and a output series inductor for higher bandwidth. The 2:1 MUX IC (Fig. 5) consists of a master-slave flip-flop (MS-FF), a master-slave-master flip-flop (MSM-FF) and a multiplexer stage (MUX 2:1). The data streams D1 and D2 are multiplexed by the 2:1 MUX stage to get a 40-Gb/s data stream.



(a) 2:1 MUX (b) 1:2 DEMUX

Fig. 5. 40 Gb/s 2:1 MUX and 1:2 DEMUX block diagram [18].

The 1:2 DEMUX IC (Fig. 5) consists of two MS-FFs and output buffers (BUF). The MS-FFs are clocked at 20 GHz.



(a) 2:1 MUX (b) 1:2 DEMUX

Fig. 6. 40 Gb/s 2:1 MUX and 1:2 DEMUX chip micrograph, chip size: 0.63 x 0.47 mm^2 each [18].

To sample every bit of the 40 Gb/s input data, the clock of one MS-FF is in phase while the other one is inverted. A separate buffer for each output decouples the MS-FFs from the 50-Ω load. The buffers use inductive peaking. The MUX and DEMUX each have a chip size of 0.63 x 0.47 mm^2. Fig. 6 shows a chip micrograph of the 40 Gb/s MUX and DEMUX.

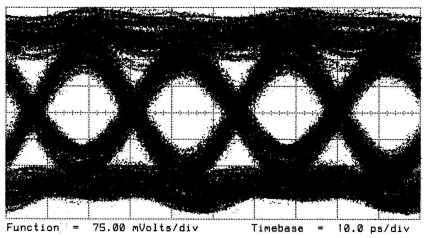
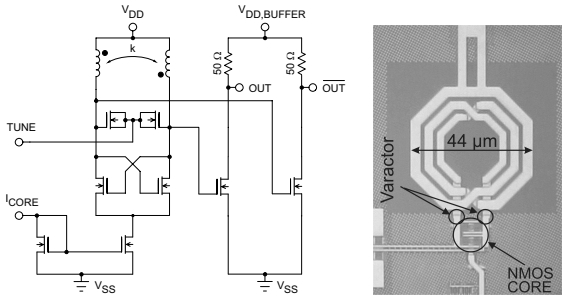


Fig. 7. 40 Gb/s measured eye diagram of 2:1 MUX output (differential signal) [18].

The MUX is tested with two pseudo-random bit sequences (PRBS of 2^7-1). The input voltage swing is 2 x 400 mV$_{pp}$. The sinusoidal clock signal has a voltage swing of 2 x 450 mV$_{pp}$. Fig. 7 shows the measured eye diagram of the differential output signal at a data rate of 40 Gb/s. The measured eye opening is 2 x 100 mV on an external 50 Ω load. The MUX draws 66 mA at 1.5 V. The demultiplexer is tested with a 40 Gb/s input data stream with 2 x 250 mV$_{pp}$ input signal voltage swing. The sinusoidal clock signal has a voltage swing of 2 x 450 mV$_{pp}$. The measured 20 Gb/s output eye opening of the DEMUX at the differential output Q1 is 2x150 mV. The 1:2 DEMUX draws 72 mA at 1.5 V.

IV. A 51 GHz CMOS Low Power VCO

A fully integrated 51 GHz VCO is implemented in 0.13 μm standard CMOS process with 6 metal levels and low-k dielectric [19]. The schematic diagram and the layout of the oscillator is shown in Fig. 8. In order to optimize the circuit for highest frequencies and lowest power, a global optimization of the active core, integrated coil and 50 Ω-output stage has been performed. The power consumption of the core is as low as 1 mW at 1 V supply voltage due to the optimized high-inductance tank. The tuning range is 1.4 GHz. The measured phasenoise is -85 dBc/Hz at 1 MHz offset from the 51.6 GHz carrier (Fig. 9).



(a) VCO schematic (b) VCO layout

Fig. 8. 51 GHz VCO schematic diagram and core layout [19].

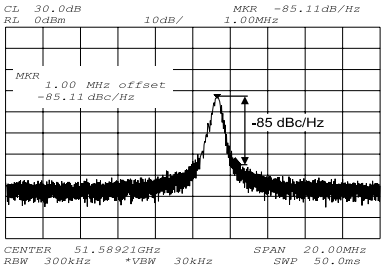


Fig. 9. Measured VCO spectrum and phasenoise at 1 V power supply, 1 mA power supply current, Vtune=1.37 V and 51 GHz[19].

V. A 98 GHz VCO in SiGe Bipolar Technology

A fully integrated VCO with a maximum operating frequency of 98.4 GHz and an output power of -6 dBm is implemented in a 200 GHz f_T SiGe bipolar technology [20]. This frequency is the highest output frequency for fundamental mode oscillators in silicon-based technologies reported so far.

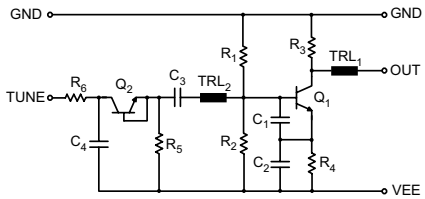


Fig. 10. Circuit diagram of the 98 GHz VCO [20].

The circuit diagram of the VCO is shown in Fig. 10. It is based on the common collector Colpitts-type oscillator. With the grounded coplanar transmission line TRL1 the impedance of the output network, comprising the pad capacitance and the 50 Ω impedance of the measurement equipment in parallel, is transformed into a low impedance at the collector of Q1. The

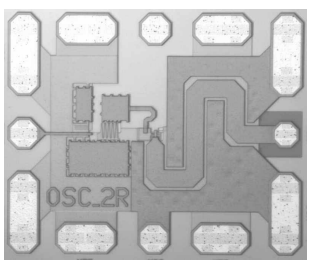


Fig. 11. 98 GHz VCO (550 μm $\times$ 450 μm) [20].

resonator consists of a transmission line TRL2, a capacitor

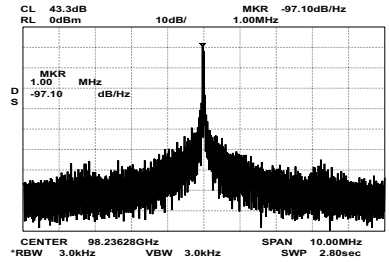


Fig. 12. Measured 98 GHz VCO output spectrum [20].

C3 and a diode-connected transistor Q2. The collector-base capacitance of Q2 is used as varactor in order to tune the oscillator's frequency. For biasing the resistors R1 to R5 are used. In Fig. 11 the chip photograph of the VCO is shown. The chip size is 550 μm $\times$ 450 μm. The oscillator operates with a supply voltage of -5 V. This leads to a total current consumption of 12 mA at an emitter current density of 6 mA/μm^2. Fig. 12 shows the output spectrum of the oscillator. The excellent phase noise performance at a frequency offset of 1 MHz is -97 dBc/Hz. Due to the losses in the measurement setup the output power is about 3 dB higher than the reported values in Fig. 12, so the output power is about -6 dBm at 98 GHz.

VI. A 86 GHz Static Frequency Divider in SiGe Bipolar Technology

The static frequency divider has a divide ratio of 32 and consists of five master-slave flip-flops (Fig. 13) [21]. The

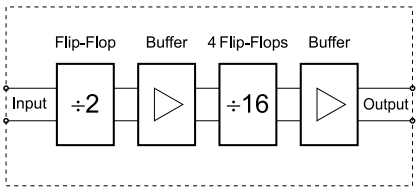
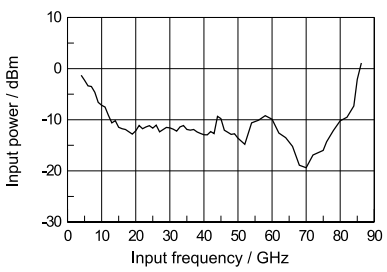


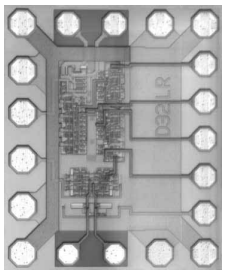
Fig. 13. 86 GHz static divider block diagram [21].

input signal is applied to the first divider stage via a pair of emitter followers. The first master-slave stage determines the maximum operating frequency of the frequency divider. This stage uses two cascaded emitter followers to achieve the highest possible operating frequency. The transistors in the first latch operate at a current density of 7 mA/μm^2. The first flip-flop is followed by a buffer consisting of a differential amplifier and emitter followers. The last divider stage is followed by an output buffer which is designed to provide an output voltage swing of >2x250 mVpp at an external 50 Ω load. Measurements were performed on wafer with a single-ended input signal. The complementary input was left unconnected. Operating with a supply voltage of -5 V the static frequency divider consumes 180 mA. Fig. 14(a) shows the measured input sensitivity.

The circuit operates up to a maximum input frequency of 86.2 GHz. Fig. 14(b) shows a chip photograph of the static frequency divider. The chip size, which is determined by the pad frame, is 550 μm x 450μm.



(a) Input sensitivity



(b) Chip photograph

Fig. 14. Input sensitivity and chip photograph of the 86 GHz static frequency divider (size: 450 μm x 550μm) [21].

VII. A 110 GHz Dynamic Frequency Divider in SiGe Bipolar Technology

The dynamic frequency divider is based on the principle of regenerative frequency division [21]. Fig. 15 shows the block diagram. The input signal is applied to a mixer which

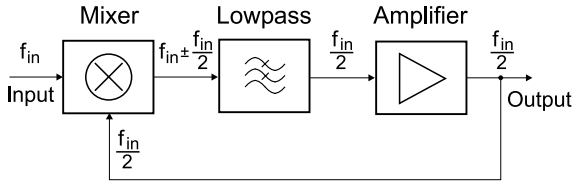
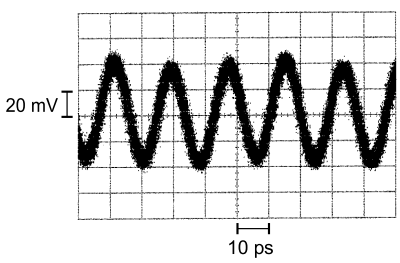
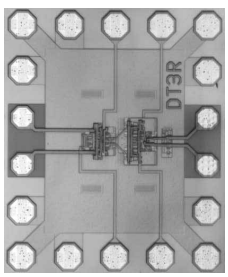


Fig. 15. Regenerative frequency division [21].

is followed by a low-pass filter and an amplifier. The output signal is fed back to the second mixer input. Three emitter follower stages are used in the feedback path of the mixer to obtain a high gain bandwidth. The output signal, which is then applied to a buffer amplifier, is taken from the first emitter follower stage. The two-stage buffer amplifier serves as limiter to make the output signal independent from the divider input amplitude. The dynamic frequency divider was measured on wafer using 1 mm coaxial probes. Input signals with frequencies up to 50 GHz were generated by a microwave generator while millimeter-wave source modules and waveguide-to-coax adapters were used at frequencies above 50 GHz. The dynamic frequency divider operates with a supply voltage of -5 V at a total supply current (including the output buffer) of 62 mA.



(a) Divider output signal (fin = 110 GHz)



(b) Chip photograph

Fig. 16. Single-ended output signal and Chip photograph of the 110 GHz dynamic frequency divider (chip size: 450 μm x 550μm) [21].

The divider operates up to 110 GHz which is the highest frequency our measurement equipment provides. With a reduced supply voltage of -4.5 V the circuit still operates up to 110 GHz while consuming only 225 mW. The single-ended output amplitude at 110 GHz input frequency is 80 mVpp (Fig. 16(a)). Fig. 16(b) shows the chip photograph of the dynamic frequency divider.

VIII. Conclusion

Finding the right match between circuit techniques and fabrication-process technology is a major issue to push the circuit performance to the frequency limits. We have presented key circuits for communication systems up to 110 GHz operating frequency. This record benchmark performance demonstrates the high-speed and low-power potential of state-of-the-art CMOS and SiGe bipolar technologies.

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