Optimum design of a new predistortion scheme for high linearity K-band MMIC power amplifiers

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ABSTRACT

A novel predistortion approach well suited for MMIC design is discussed. The theoretical analysis shows third-order intermodulation product (IMP3) cancellation independent of the specific technology exploited for implementation and of the detailed behaviour of the power stage nonlinearity; further improvements can be obtained through optimization. The active stages of the predistorter are modeled through a nonlinear describing function, which can be experimentally characterized through standard LS S-parameters measurements. The predistortion scheme has been implemented within the Agilent ADS environment and applied to the linearity optimization of a power amplifier stage. In accordance with theoretical results, significant improvement in the linearity of the Pin-Pout is demonstrated together with IMP3 reduction. A sensitivity analysis on the optimization parameters is also presented, showing that this approach is robust and well suited for circuit design.

INTRODUCTION

IMP3 reduction is a key design challenge for RF and microwave power amplifiers exploiting broadband modulation schemes. Several approaches have been proposed to achieve high carrier to IMP3 ratio (CIMR) in high-linearity power amplifiers. A well known technique exploits a predistortion stage, characterized by an LS gain behaviour aimed at exactly or partly compensating the gain compression of the power stage. The predistortion stage design is critical, as it usually involves two circuit branches which combine signals with proper phase shifts, see e.g. [1, 2]. A delay element is therefore required in one branch to compensate for the delay in the active device; the delay element design can be difficult, above all when the operating frequency is high enough (e.g. in K band) and the amplifier bandwidth is moderately wide.

Two relevant predistorsion schemes [3, 4] exploit active FET devices in the two branches, one operating in linear condition and the other in nonlinear regime. In [3] the nonlinear active device, is a low-power (scaled-down) version of the power stage, while the other branch includes a generic linear amplifier. In [4] the two active devices are built with the same technology and properly scaled to achieve different power compression levels in the two branches.

In this paper we propose a similar circuit scheme, where both circuit branches include an active device (amplifier). As opposed to [3, 4] the two active devices are the same thus making the delay element unnecessary and the different compression in the two branches is achieved by means of attenuators. Furthermore the two active elements of the predistorter have device periphery properly scaled down with respect to the power stage, so that the whole linearized amplifier can be reliably designed in MMIC form. With respect to [3] the stucture of the linear and nonlinear branches are completely specified allowing for a theoretical analysis in order to extract optimum design parameters for IMP3 minimization and circuit optimization. This predistortion method can be applied to very high frequency amplifiers where other linearization techniques, such as feedforward schemes, are not yet well established.

The paper is structured as follows: the nonlinear model employed for the theoretical analysis is introduced; then, the linearization scheme is described and the theoretical analysis is presented so as to extract the predistorsion stage design criteria. The circuit scheme is verified, at least at a CAD level, through circuit simulations, obtained implementing the model within the RF CAD tool ADS by Agilent. Some remarks will be finally devoted to the sensitivity analysis on some crucial parameters for design optimization.

DESCRIBING FUNCTION MODEL

The input signals for amplifier IMD analysis are normally narrow-band modulated signals, so that the incident wave at the amplifier input can be expressed in the form $Re\{a_{iP}(t)e^{j2\pi f_0 t}\}$, where f_0 is the carrier frequency and $a_{iP}(t)$ the

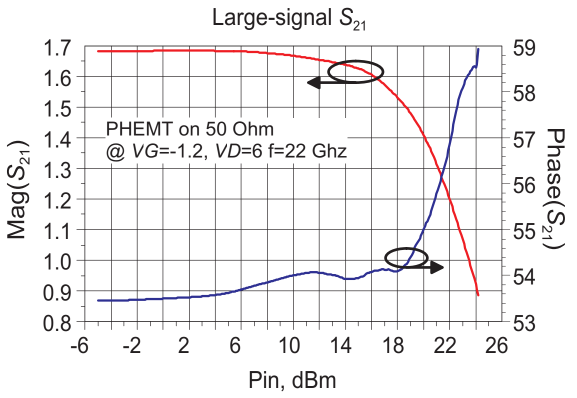

Figure 1: LS S_{21} from the PHEMT FMM model with $V_{GS} = -1.2$ V, $V_{DS} = 6$ V and $f = 22$ GHz.

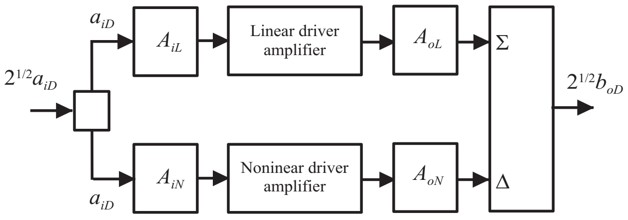

Figure 3: Circuit predistortion scheme.

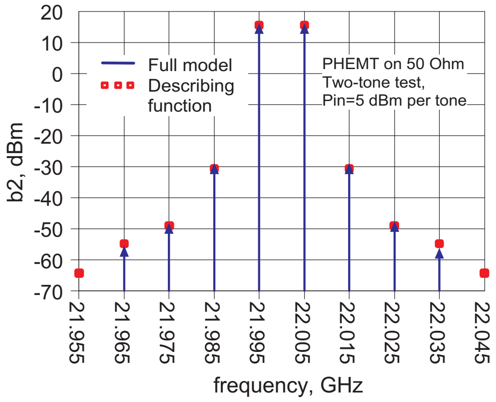

Figure 2: Comparison of the spectra around the center frequency (22 GHz) for two tone excitation (tone spacing 10 MHz) between the FMM and the describing function based model.

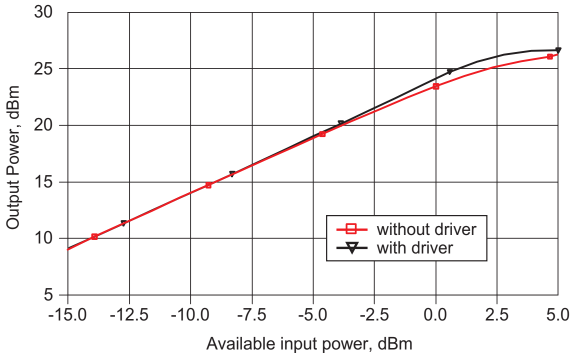

Figure 4: Output power VS available input power of the total amplifier with the predistortion stage, compared to the one without linearization scheme.

complex modulation envelope. In particular, the typical test signal made up of two tones at frequencies f_a and f_b can easily be expressed as an equivalent modulated signal with carrier frequency $f_0 = (f_a + f_b)/2$, whose complex modulation envelope $a_{iP}(t)$ is slowly time-varying when the two-tone frequency spacing $f_a - f_b$ is small. In such conditions, the relationship between the complex modulation envelopes of the amplifier input and output waves, $a_{iP}(t)$, $b_{oP}(t)$, is almost memoryless, so that the in-band amplifier response (out-of-band distortion products are not considered) can be described by the algebraic equation [5]:

$$b_{oP}(t) = F_P(|a_{iP}(t)|^2)a_{iP}(t)$$

$F_P(|a_{iP}(t)|^2)$ is the system *describing function* which completely characterizes the amplifier response to any narrow-band modulated signal with carrier frequency f_0, and is a complex non-linear function of the envelope instantaneous input power $|a_{iP}(t)|^2$. Notice that b_{oP}/a_{iP} is an even function of $|a_{iP}|$, as it can be rigorously shown by Volterra analysis by considering only in-band output frequency components.

Let us separate the linear and nonlinear part of F_P, $F_P = G_P + F(|a_{iP}|^2)$, where G_P is the small-signal complex gain of the power stage, while $F(|a_{iP}|^2)$ is a function such that $F(0) = 0$. The power stage input-output characteristics can be thus written as: $b_{oP} = G_P a_{iP} + F(|a_{iP}|^2)a_{iP}$. In order to evaluate third order IMP's from the above formulation, a power series expansion of the describing function up to the first order is required, i.e. $F(|a_{iP}|^2) \sim F_1 \cdot |a_{iP}|^2$.

The function $F(|a_{iP}|^2)$ can be easily extracted experimentally, by means of large-signal complex gain measurements (i.e. large-signal S_{21}) for different amplitudes of a sinusoidal input signal at the carrier frequency f_0. It will be shown that the exact behavior of the describing function is not critical for predistortion design. As an example we consider a PHEMT device from Alenia Marconi, modelled in LS condition by the FMM (Finite Memory Model) [6] and extract the describing function as a function of the input power: the amplitude and phase of the LS S_{21} in a class A working point and operating frequency of 22 GHz are shown in Fig. 1. A two-tone simulation of the PHEMT response was performed and compared with the describing function model. The capability of the model to correctly reproduce high order intermodulation is shown in Fig. 2.

For the predistortion stage, we use a driver amplifier based on the same device as the power stage, but with a scaled-down periphery. Suppose the power amplifier has a total periphery w_P and the driver a total periphery $w_D < w_P$; then, defining the scale factor $k_{DP} = w_D/w_P < 1$, the output signal of the driver will be scaled down with respect to the output signal of the power stage by a factor k_{DP}. Anyway, since the input power is also scaled down, the gain will be the same (with proper input and output matching). However, the driver will saturate at a lower input signal. In other words we can postulate the following scaling rule:

$$b_{oD} = G_P a_{iD} + k_{DP} F\left(\frac{|a_{iD}|^2}{k_{DP}^2}\right) a_{iD}$$

PREDISTORSION SCHEME THEORY AND OPTIMUM DESIGN

The predistortion scheme is shown in Fig. 3. The input power is split into two circuit branches, each including a driver amplifier and two attenuators. The *linear* driver amplifier is driven at low input power through the (high-attenuation) attenuator A_{iL}; its output is fed, through the attenuator A_{oL}, into the 180^o hybrid (sum port). The *nonlinear* driver amplifier is driven at high input power through the (low-attenuation) attenuator A_{iN}; its output is fed, through the attenuator A_{oN}, into the 180^o hybrid (difference port). It will be shown that some of the attenuators are redundant. Notice also that, for the sake of simplicity, a global input to the splitter is assumed as $\sqrt{2}a_{iD}$ rather than a_{iD}.

The analysis of the stage is as follows. Assuming the upper branch as strictly linear, the input at the hybrid sum port is simply $a_\Sigma = A_{oL} G_D A_{iL} a_{iD}$. The difference port input is, from the analysis of the lower branch:

$$a_\Delta = A_{oN} G_D A_{iN} a_{iD} + A_{oN} k_{DP} F\left(\frac{|A_{iN} a_{iD}|^2}{k_{DP}^2}\right) A_{iN} a_{iD}$$

Thus, the driver output signal is $\sqrt{2}b_{oD} = a_\Sigma - a_\Delta$. We can further evaluate the output of the power stage assuming $a_{iP} = \sqrt{2}b_{oD}$. By defining:

$$G_\Sigma = A_{oL} G_D A_{iL} \qquad G_\Delta = A_{oN} G_D A_{iN} \qquad \text{and} \qquad k_\Delta = A_{oN} k_{DP} A_{iN}$$

the final power stage output signal is:

$$b_{oP} = G_P y + F(|y|^2) y$$

where:

$$y = (G_\Sigma - G_\Delta)\, a_{iD} - k_\Delta F\left(\frac{|A_{iN} a_{iD}|^2}{k_{DP}^2}\right) a_{iD}$$

By first-order power series expansion of the function F, one finds that an *exact* cancellation of the third order terms in b_{oP} is achieved by:

$$G_P k_\Delta = G_\Sigma - G_\Delta \qquad \text{and} \qquad |G_\Sigma - G_\Delta| = A_{iN}/k_{DP}$$

The above condition is satisfied by choosing the attenuation $A_{iN} = 1$ and $A_{oL} = 1$ and:

$$A_{oN} = \frac{1}{k_{DP}^2 |G_P|} \qquad A_{iL} = \frac{1 + k_{DP}}{k_{DP}^2 |G_P|}$$

Notice that A_{iL} is always greater than A_{oN}. Furthermore, it can be shown that this assumption also partly cancels the fifth-order output nonlinearity, thus further decreasing IMP3's.

In order to provide a first CAD validation of the approach, the nonlinear model and circuit scheme have been implemented in the Agilent ADS circuit simulator. A power amplifier is considered, composed of three cascaded stages exploiting the PHEMT device discussed in the previous section, with proper impedance matching for optimum gain. A driver stage has been designed by scaling down the amplifier perifery according to the previous analysis. The Pin-Pout characteristics of the total amplifier with the predistortion stage are compared in Fig. 4 to the amplifier with no linearization scheme. The gain compression of the total power amplifier is shown in Fig. 5 with and without predistortion stage, showing significant improvement in the output power at 1 dB compression for the linearized amplifier. Concerning IMP3's and CIMR, the optimum predistorsion scheme provides, on a 20 dB output power range, a 10 dB improvement with respect to the power amplifier only. Some improvements can be achieved by tuning the attenuation around the optimum value and adding a small phase delay. By optimizing such parameters for *each* value of the output power the results shown in Fig. 7 are obtained, with a further 10 dB CIMR improvement; the local optimum values are plotted in Fig. 8. Since both attenuation and phase delay cannot be locally tuned versus input power in practice in a variable output power system, a global average optimum was sought, which takes place at an attenuation 0.25 dB larger than the theoretical optimum and for a 1° phase delay, see Fig. 7; however, the global improvement achieved from 10 to 20 dBm output power is small.

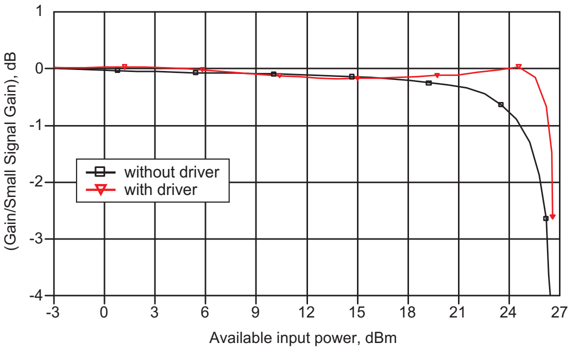

Figure 5: Gain compression VS available input power, showing the improvement in the 1 dB compression point in the linearized amplifier. The gain behavior of the predistortion stage is also shown.

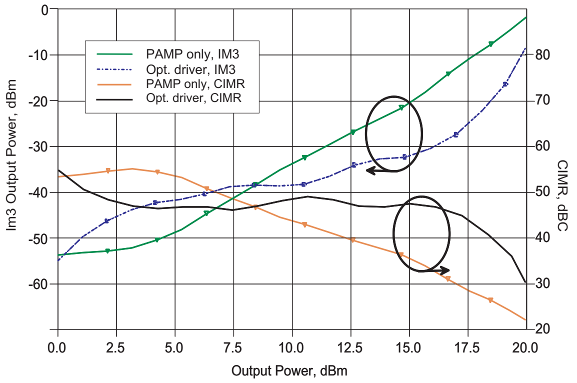

Figure 6: IMP3 characteristic and CIMR for the amplifier stage with and without predistortion driver.

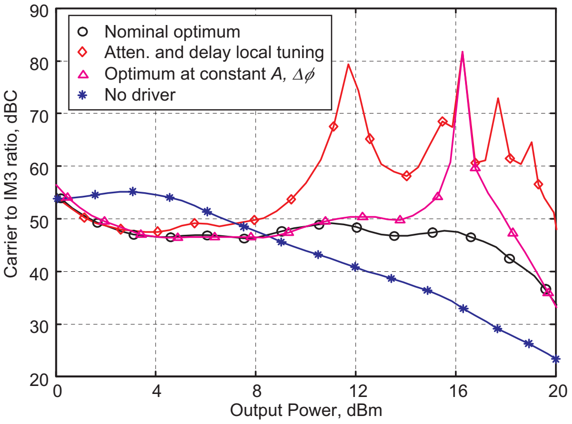

Figure 7: CIMR versus output power by optimizing the attenuation and introducing a phase delay.

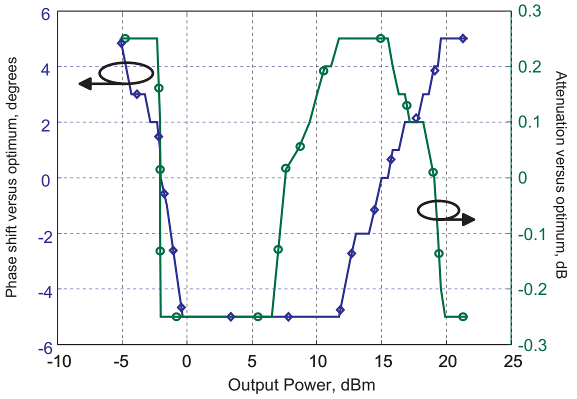

Figure 8: Local optimum attenuation and phase delay (with respect to theoretical optimum) versus output power.

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