10 W High Efficiency 14V HBT Power Amplifier for Space Applications

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Abstract : *This paper presents the first development of a space-borne power amplifier using the recently developed high breakdown, high Power HBT HB20S process of UMS. The inverse F class Hybrid Power Amplifier has been designed using intensive simulation methods developed at Alcatel Space for MMICs, allowing to reach very high performances without manual tuning. The results 10 W / PAE > 65% obtained with a single chip at 1.5 GHz demonstrate the capability of the process to handle with very high power densities and efficiencies.*

I) INTRODUCTION

For the last few years, the GaInP/GaAs HBT power technology has become mature enough to be compatible with on board space applications [1]
Recent developments around a very high power HBT process (HB20S) at UMS [2] has given an intermediary short term schedule for the use of high breakdown voltage components before wide bandgap component industrial standardisation. The fundamental characteristics of this process are a Vce breakdown = 31 V, and a Vcb breakdown = 65V.
The application of such a very high power process in next upcoming spatial navigation programs like Galileo, which are very demanding on solid state high power amplifiers, could be of particular interest.

II) TOPOLOGY OF HBT DEVICES

The devices used for this work are based on a fishbone type elementary cell of 16 fingers of 2x70µm² emitter area. The corresponding layout is given in Figure 1.

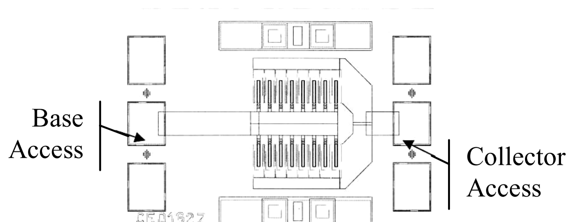

Figure 1 : Layout of a 16x(2x70µm²) cell

The discrete power bar mounted in the hybrid circuit described in this paper, is composed of 4 elementary cells in parallel sharing an single 30 µm thick thermal drain connected to emitter fingers at the upper side and joining the backside metal through via holes. In front of each elementary cell, a pre-matching circuit has been included directly on GaAs (Figure 2). The substrate thickness is 100µm.

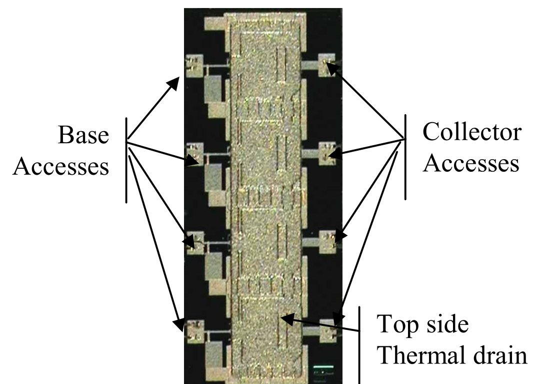

Figure 2 : Top side view of the Power chip

III) LOAD PULL AND DESIGN METHOD

An electrothermal model of the 16x(2x70µm²) elementary cell has been extracted using pulsed I/V and S parameters, obtained for different base plate temperatures [3].
The bias point for an elementary cell has been chosen at Vce=14 V / Ice =50 mA, in deep AB class and not in B class to preserve small signal gain. The base is biased using a mix bias method including a series resistor and a voltage source.
Despite the possibility to bias at a voltage superior to 20V, the 14V value has been chosen to limit junction temperature. The component is consequently used in a particularly safe area, particularly attractive for space applications.
The optimum load conditions have been determined for an optimum PAE using load and source pull simulations at fundamental frequency f0 but also at second harmonic 2f0. The optimum impedance found (Figure 3) show a remarkably high value at f0 (easier to match to 50 Ω) as a direct consequence of the high voltage collector bias point, and a quasi open circuit at 2f0 leading to inverse F class [4].

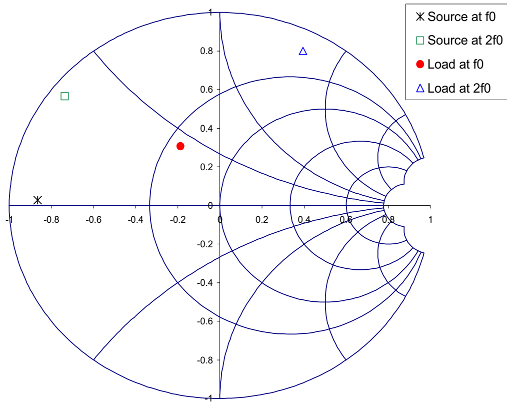

Figure 3 : Optimum Load / Source Impedance

Input and output matching circuits are made with a high dielectric constant material to minimise losses as well as dimensions.
The hybrid amplifier has been first simulated using standard equivalent elements of a commercial simulator microstrip library. Then, to overcome the library limitation for the high dielectric constants, a complete quasi 3D electromagnetic simulation [5] of the matching circuits has been performed.
The simulated non linear results given in Figure 4 show for 2 dB of gain compression over the frequency range 1.525 / 1.625 GHz a module output Power > 10 W, a module PAE > 62% (peak to 65%) and an associated Gain >13.2 dB (peak to 13.75 dB). The resulting power density at Vce=14V is 2.23 W /mm corresponding to 6 times the power density of a typical HFET L band power amplifier [6].

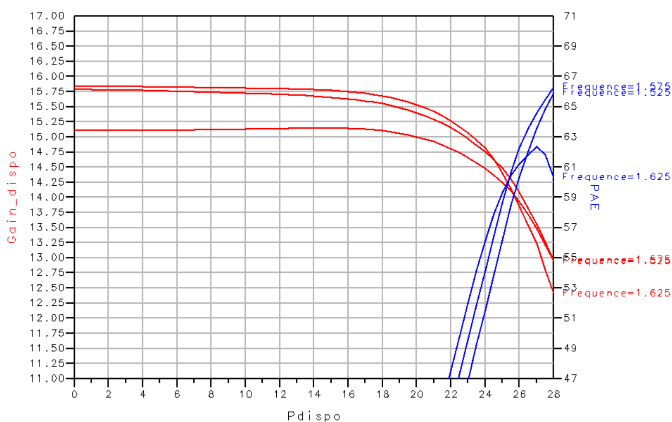

Figure 4 : Simulated performances

IV) TIME DOMAIN WAVEFORMS

One of major concern for space application is the reliability of the equipment manufactured. For a power amplifier, the critical part is the transistor whose intrinsic (technological) reliability characteristics shall be satisfactory (typically MTTF $>10^6$ Hours). The time domain visualisation of voltage and current waveforms gives an evaluation of the dynamic stress applied to the component and shall respect the normalised derating (i.e. 75%) of foundry maximum ratings. For the High breakdown voltage HB20S process, UMS gives the following static maximum ratings, for the collector to base breakdown voltage : Vcb_B =65 V, and for the collector to emitter breakdown voltage Vce_B=31 V.

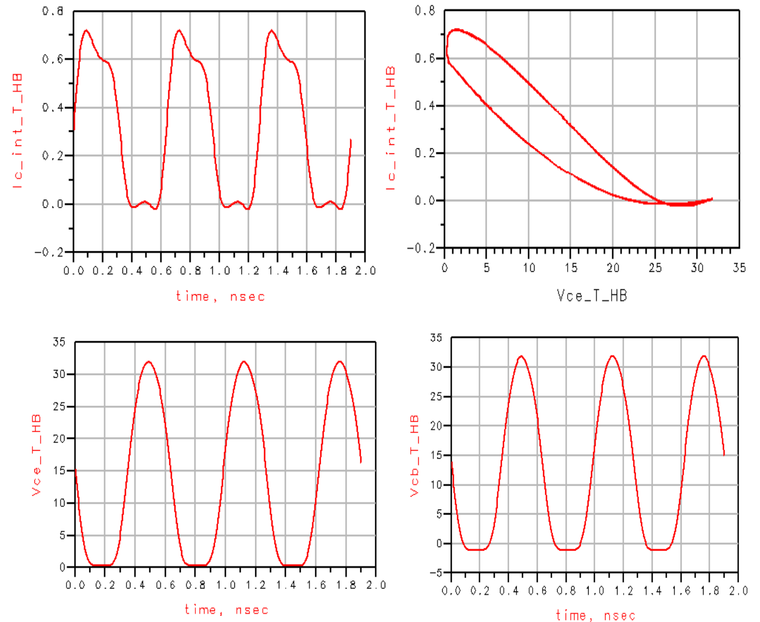

Figure 5: Load Pull Simulated Time Waveforms (P2dB)

As it is shown in Figure 5 (Load Pull simulated waveforms corresponding to 2 dB of HPA gain compression), the Vce dynamic voltage with a peak value of 31V remains inferior to the static Vce_B as well as for the Vcb waveform with an absolute peak to 33V to compare with the 65 V of Vcb_B. This graphs show an important margin (better than the rated 25%) to the most critical value Vcb_B for reliability. The static Vce maximum rating is respected.
As a second comparison, the Figure 6 shows the same waveforms (for 2 dB of gain compression), at 3 frequencies (upper, center and lower in the bandwidth), simulated for the transistors with its matching networks inside the HPA. As it is shown the same margin versus Vcb_B and Vce_B are obtained.

V) RF CW POWER MEASUREMENTS

The realised amplifier has been measured using CW signal in a slightly shifted band (70MHz) compared to simulations. The measurement results (Figure 7) show at least 10 W of output power for 2dB of gain compression and an associated PAE >64.5 % (peak to 66%) over 50MHz bandwidth for an associated Gain > 13 dB (peak to 13.6dB). The very good correlation between simulated and measured performances show the validity of the transistor model and design method.

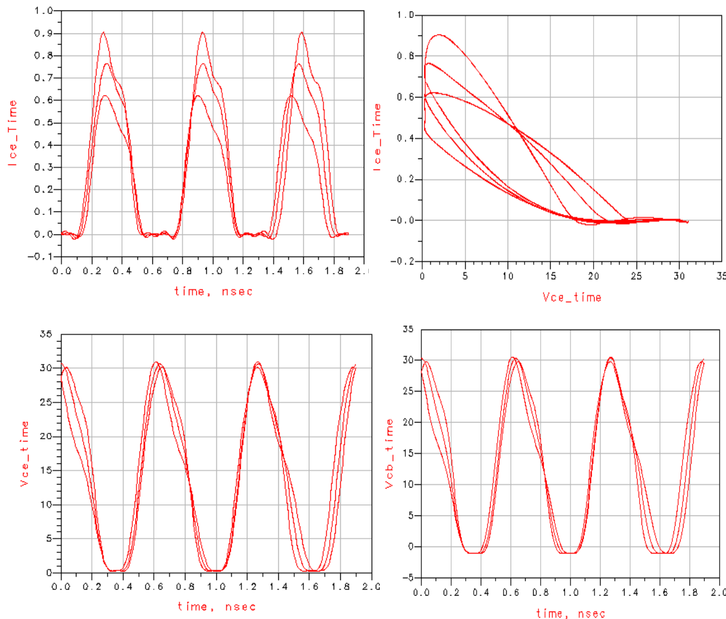

Figure 6: Designed HPA Simulated Time Waveforms (P2dB)

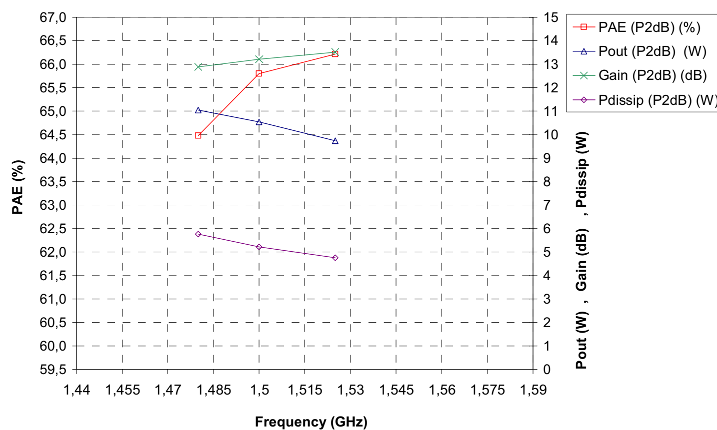

Figure 7 : CW Power module Measurements

These performances, reported between input and output plans of a 50Ω module (Figure 12) without any deembeding of the losses due to the test jig or SMA connectors, are, as far as we know, in the state art of the 10W single chip category. Previous work on High Voltage Breakdown HBT reported 20W and a PAE = 62% at a transistor level for a 28V bias [7].

VI) RF TWO TONE MEASUREMENTS

Compared to the typical performances of a HFET module commonly used in space applications [6], the 2 Tone linearity of the high Voltage HBT power module shows a particular improvement especially for high compression zone. Typically as it is shown in the Table 1, the improvement compared to a HFET could be up to 4dB for Δf=10 MHz at –3dB of IBO (input power back off).

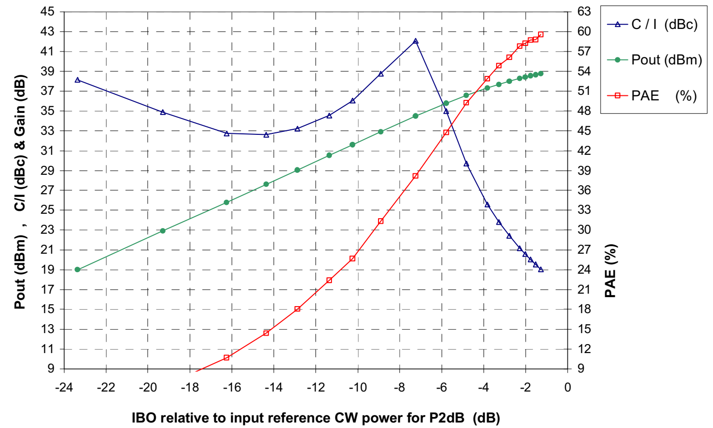

Figure 8 : 2 Tones Power module Measurement

3rd order intermod.	HBT HB20S 10W L Band	HFET C Band
IBO /CW	Δf=10MHz	Δf=10MHz
-3 dB	23.2 dBc	19.1 dBc
-10 dB	36.7 dBc	35 dBc
-17 dB	33 dBc	44 dBc

Table 1:Linearity as a function of Input BackOff

The reference input power for IBO is the input power for 2dB of CW gain compression

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VII) JUNCTION TEMPERATURE

The elementary cell and the whole packaging environment have been thermally simulated to estimate the thermal resistance as a function of base plate temperature. The graph presented in Figure 9 depicts the thermal distribution between each emitter finger (only half of the structure has been simulated for symmetry reasons). It is shown that the center fingers are the hottest, and depending on the position in the finger as well as the finger considered, the thermal gradient can reach 10 °C (edge effect).

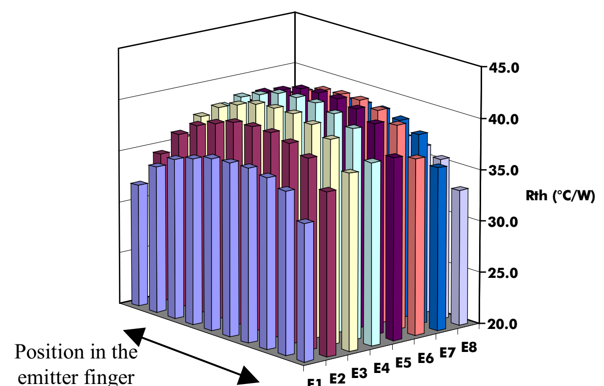

Figure 9 : Thermal distribution between 8 emitter fingers of the elementary cell

On the basis of these results, the evolution of Rth has been plotted versus base plate temperature, taking into account the max temperature or the average temperature over an elementary cell.

As it is shown in Figure 10, the thermal resistance of the elementary cell reaches about 42°C/W for a chip bottom temperature of 80°C. The resulting Rth for the complete power chip is 10.5°C/W, as low as the value reported in [7].

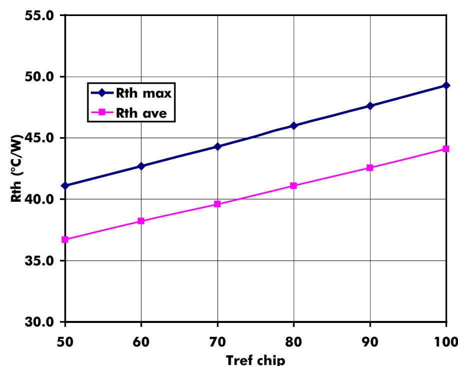

Figure 10 : Rth of an elementary cell

For the 60°C base plate temperature corresponding to the Galileo L Band specification temperature, the worst case junction temperature including the entire equipment packaging thermal resistance (up to calloduc) could be calculated this way :

Signal	Max Module dissipated power	Transistor dissipated. Power (matching subtracted)	Delta T due to packaging (up to chip bottom)	Tj
CW	5.8W	4.85 W	22.4 °C	131°C
2 Tones	4.65W	4 W	18.7 °C	119 °C

Figure 11 : Junction temperature Estimation

VIII) CONCLUSION

The very attractive 10W / 66% obtained thanks to high breakdown voltage HBT make them very interesting in the frame of very high power amplifier applications. To be completely compatible with a space industrial application, further improvements around the junction temperature should be engaged to reach the maximum 115°C for a 10W output power with the real case of application signal.

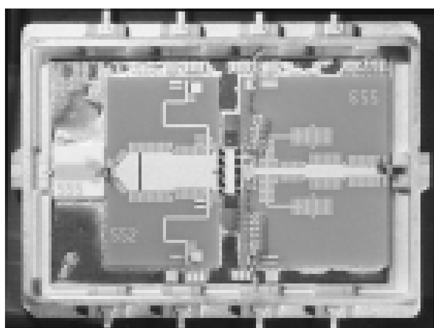

Figure 12 : Photograph of the 10W Module

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