

# A Chip-Scale Packaged Amplifier MMIC using Broadband Hot-Via Transitions

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**Abstract** — The performance of RF *hot-via* transitions for use in chip-scale package (CSP) MMICs are presented. This is illustrated with the realization of a low noise amplifier MMIC using optimized *hot-vias*. Based on our standard 0.25- $\mu\text{m}$  GaAs low-noise PHEMT process, with BCB coating and backside metallization, this 2-stage low noise microstrip amplifier mounted with bumps on a carrier substrate achieved a linear gain of 15 dB over the 15- to 32 GHz frequency range. To the author's knowledge, this is the first demonstration of chip-scale packaged active MMICs using *hot-via* transitions.

## I. INTRODUCTION

The trends of microwave and millimeterwave ICs is toward cost effective packaged products, compatible with Surface Mount Device (SMD) assembly line [1]. Among the number of existing SMD approaches for microwave devices (flange mount, lead frame etc.), one of the most promising solution might be the Chip Scale Package (CSP) MMIC. CSP generally refers to an encapsulated MMIC whose the total volume is only 1.5 times bigger (or less) than the bare die, and that have RF and DC interconnects compatible with PCB line resolution. CSP is cost effective since it is a collective wafer-level packaging process that includes, in one step, both the package and IC assembly, without wire bonding. Wires are indeed replaced by bumps in combination with coplanar flip-chip or hot-via techniques. Whereas the flip-chip approach in combination with coplanar MMICs provides good RF and thermal properties, even up- and above the millimeter wave range [2], most MMICs are still designed with the conventional microstrip technique.

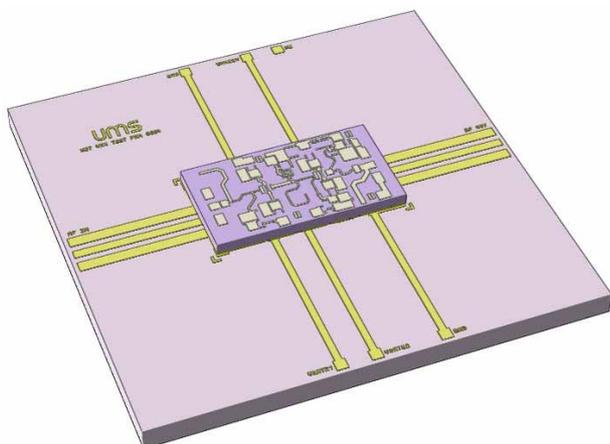


Fig. 1: Example of MMIC DC-, Ground- and RF connected with hot-via to a carrier plate with coplanar lines.

Perhaps one of the most promising alternative to flip-chip technology, especially for power MMICs is the “*hot-via*” concept [3-5]. With the “*hot-via*”, the chip is mounted face-up on a carrier, by mean of bumps connecting the backside on the carrier substrate (AlN, Al<sub>2</sub>O<sub>3</sub>, LTCC, etc.). As shown in figures 1 and 2, the front-side RF and DC pads, are connected to the backside and the bump interconnects using via-holes (Fig. 2). In addition to its inherent compatibility with microstrip MMICs, the *hot-via* mounting provides simultaneously reproducible electrical- (RF, DC and Ground), thermal- and physical attachment of the MMIC to the “*outer world*”, alleviating many technical problems like bond wire parasitic inductance, additional mounting steps, chip alignment. Furthermore, this cost effective technique can be used with SMD automated assembly lines, and the MMICs can be visually inspected after mounting. Yet another advantage of the *hot-via*, is that the backside ground metallization pattern acts as a shield against any structure underneath; therefore de-tuning effects or spurious resonance are eliminated compared to flip-chip coplanar mounting [6].

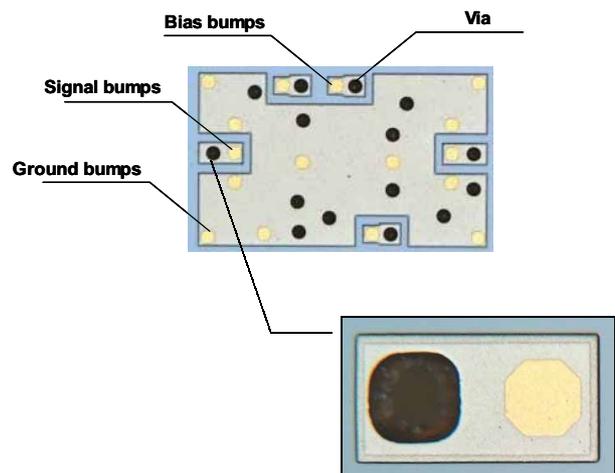


Fig. 2: Backside chip photograph of a low noise amplifier with RF and DC hot-vias, and locations of the bumps.

## II. CHIP SCALE PACKAGE PROCESS

The different MMIC examples reported in this paper are fabricated with the UMS PH25 PHEMT production process, using 0.25- $\mu\text{m}$  Aluminum T-gates on 4” wafers, with 100- $\mu\text{m}$  thick GaAs substrate and standard via-hole

technology (30- $\mu\text{m}$  front-side diameter). The MMICs are fully dielectrically coated with a BCB to ensure a collective wafer-level front-side encapsulation. The process is standard up to the backside gold plating. Afterwards, additional process steps include:

- AuGe/Au plating
- 1- $\mu\text{m}$  Ni plating, acting both as etching mask for the gold and as diffusion barrier for the SnPb bumps
- 20- to 50-nm evaporated gold for de-wetting and bump soldering area
- 70- $\mu\text{m}$  height SnPb plated bumps
- front-side plastic molding (optional)

After dicing the MMICs are mounted onto a carrier plate and the bumps attached to the board lines with re-flow soldering process. At this final step, the bumps are approximately 30- $\mu\text{m}$  high with 75- $\mu\text{m}$  diameter (Fig. 3).

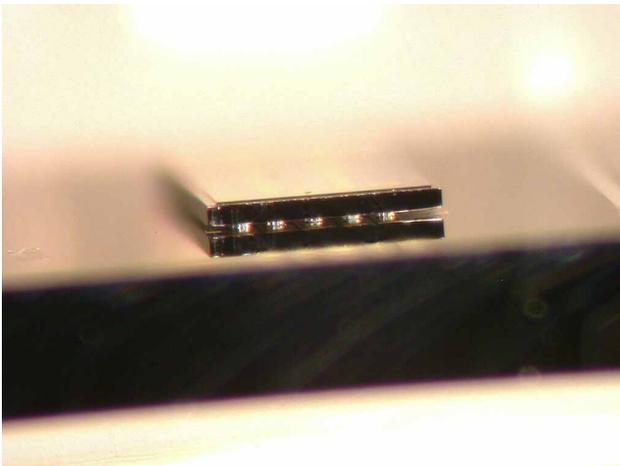


Fig. 3: Side photograph of an *hot-via* transmission line test structure mounted with RF bumps on a carrier plate.

### III. OPTIMIZATION OF RF HOT-VIA INTERCONNECTS

In order to minimize the parasitic introduced by the *hot-via* transition, as well as its amount of chip area, several RF *hot-vias* transitions were investigated and optimized in shape, size and slot width, for broadband operation. This was performed by mean of 3D electromagnetic simulations (i.e. CST Microwave Studio<sup>®</sup>). It resulted in a set of different optimized RF hot vias transitions comparably smaller than conventional front-side RF pads, with no size- or performance penalties for existing IC designs. These transitions are of two types:

1. “coplanar-like”, using ground-signal-ground via-structures (e.g. Fig. 1-5)
2. “stripline-like”, using only ground-signal via structures (e.g. Fig. 8)

They can be used either with on-board coplanar-, stripe- or microstrip lines.

Further size minimization was achieved as well, by designing RF hot-via transitions in the corner of the chip as shown in Fig. 4, and the example of Fig. 8.

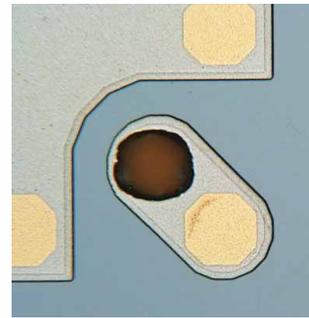


Fig. 4: Microphotograph of an RF hot-via transition placed in the corner of a MMIC.

### IV. RESULTS AND DISCUSSION

The Fig. 5 shows an example of transition test structures used for the characterization of RF hot-via and bump interconnects. It is made of on-board feed 50- $\Omega$  coplanar lines connected with bumps and hot-vias to 50- $\Omega$  microstrip transmission line on GaAs. The Fig. 6 presents the measured S-parameters for the upper transmission line test structure. As shown, while the input- and output return losses are below  $-10$  dB up to 25 GHz, the insertion loss remain below  $-2$  dB for the whole test structure, let less than 0.5 dB @ 40 GHz per single *hot-via/bump* transition, demonstrating potential use of this technique up to at least 40 GHz. The Fig. 7 presents the measured S-parameters of the shorted transmission line test structure. This element is used in the *hot-via/bump* parasitic element extraction, and allows by a relative de-embedding technique, the accurate determination of reference planes and losses.

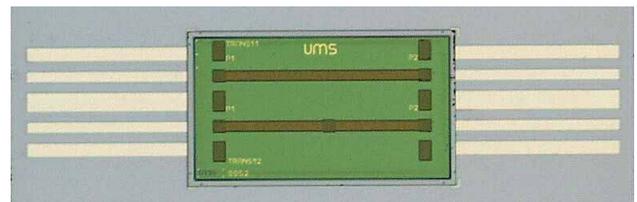


Fig. 5: Example of transmission line test structure used for hot-via + bump characterization (up: thru-line, down: short-line).

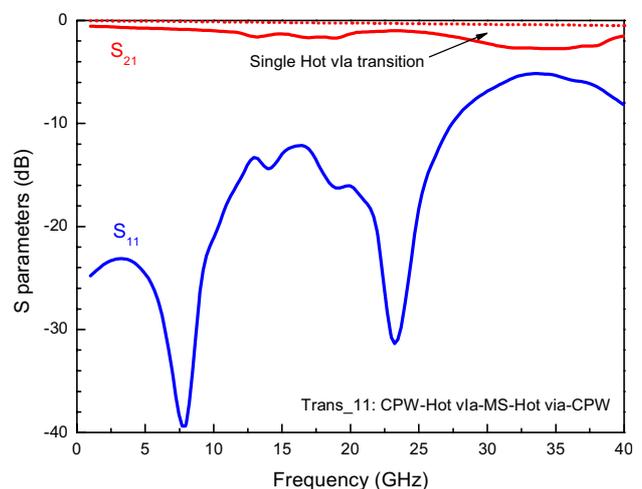


Fig. 6: Measured S-parameters of thru-line test structure (up test structure in Fig. 5).

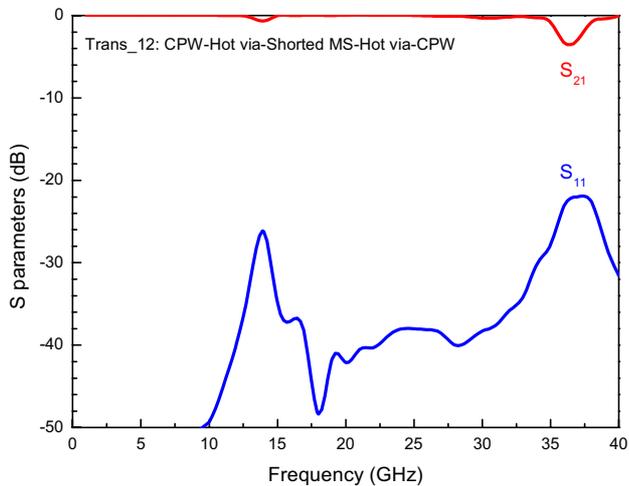


Fig. 7: Measured S-parameters of thru-line test structure (down test structure in Fig. 5).

To demonstrate that *hot-via* concept is applicable not only to passives, but to active CSP MMICs as well, the backside metallization pattern of a standard UMS product, has been modified to be compatible for different mounting with “*coplanar-*” and “*stripline-*” like hot-vias. The Cha2190 is a two-stage, self biased wide band low noise amplifier, providing typically 15-dB gain and 2.2-dB noise figure over the 20-30 GHz frequency range, for a chip size of  $1.67 \times 1.03 \text{ mm}^2$  ( $1.72 \text{ mm}^2$ ) [7]. It is worth mentioning that the size of the chip remains unchanged, and that the *hot-via* transitions are incorporated within the remaining chip area, while essentially modifying the back-side metallization pattern, and including a full BCB coating.

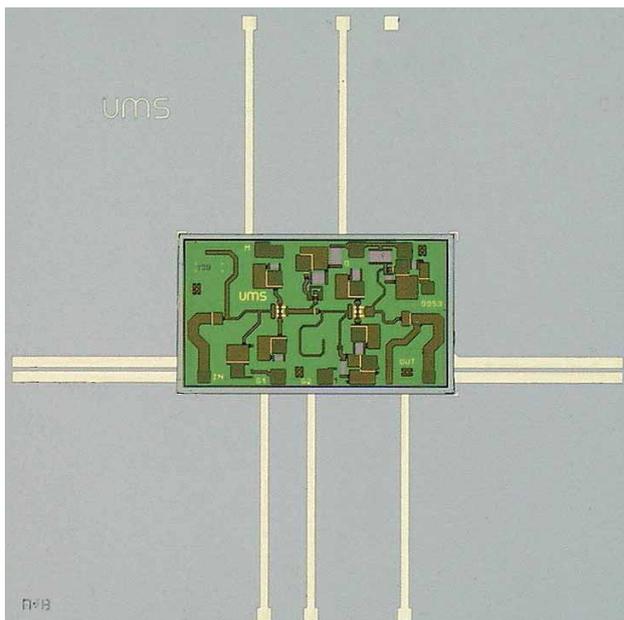


Fig. 8: Example of a low noise amplifier using *hot-via* transition mounted on a carrier plate with *striplines*.

The Fig. 8 shows an example of CSP amplifier MMIC mounted on a carrier plate with feed *striplines*, placed in the corners of the chip. The Fig. 8 shows the measured S-parameters, it demonstrates that the broadband performance of this “*hot-via/bump connected*” LNA in

CSP form, are as good as in die form, with an insertion gain for the whole test structure of 15 dB from 13- to 32 GHz, and good input- and output return losses of typically -10 dB (-8 and -6 dB max. over the bandwidth, respectively). Both “*coplanar*” or “*stripline*” hot-vias transitions exhibited very similar results in both gain and return losses.

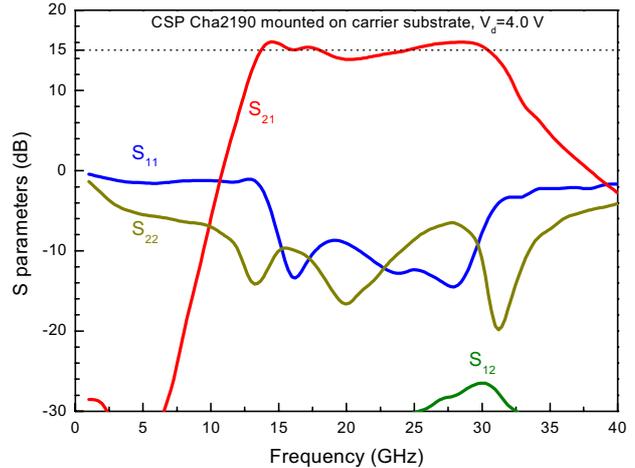


Fig. 9: Measured gain, input- and output return loss of the *chip scale package LNA* with *hot-via* transitions.

## V. CONCLUSION

These results demonstrate that with suitable optimization, the *hot-via* interconnect exhibits very good performance up to at least 40 GHz, without degrading the performance of active device MMICs. This is illustrated by the successful realization of the first SMT compatible chip-scale packaged amplifier MMIC using *hot-via* transitions. This suggests as well potential use of this technique for low cost packaging solutions up- and above the millimeter-wave range.

## ACKNOWLEDGEMENT

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