A SiGe HEMT Mixer IC with Low Conversion Loss

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***Abstract* -- The authors present the first SiGe HEMT mixer integrated circuit. The active mixer stage, operating up to 10GHz RF, has been designed and realized using a 0.1µm gate length transistor technology. The design is based on a new large-signal simulation model developed for the SiGe HEMT. Good agreement between simulation and measurement is reached. The mixer exhibits 4.0dB and 4.7dB conversion loss when down-converting 3.0GHz and 6.0GHz signals, respectively, to an intermediate frequency of 500MHz using high-side injection of 5dBm local oscillator power. Conversion loss is less than 8dB for RF frequencies up to 10GHz with a mixer linearity of –8.8dBm input related 1dB compression point.**

I. INTRODUCTION

The High Electron Mobility Transistor (HEMT) concept today offers the highest transistor cut-off frequencies combined with power capability and low noise performance. These devices are well established on GaAs and InP substrates but their relatively high production cost makes them less attractive for many consumer applications. Realizing HEMT structures on Si substrates combines HEMT performance with low cost and the possibility of integration with other Si-based technologies. Such devices use the high mobility of electrons in a two-dimensional electron gas (2DEG) in a strained Si layer. Successful realization has been demonstrated with respectable device performance [1]-[4]. A transimpedance amplifier IC using the SiGe HEMT has been reported in [5]. However, its design was not based on simulation due to the lack of models. As a consequence, the next step towards realization of integrated circuit prototypes in SiGe HEMT technology was the development of a simulation model. An empirical large-signal model has been demonstrated in [6]. Based on these prerequisites, the first SiGe HEMT mixer IC has been designed, processed and characterized. The design of an active mixer is, among other applications, well suited for demonstrating the technology's capabilities. It makes use of the transistor's high frequency- as well as low noise performance. The high linearity inherent to HEMT technology will be advantageous for good mixer linearity. Also, gain requirements are less stringent in the design of mixers.

The contribution presents simulation and measurement results of an active mixer cell designed with 0.1µm gate length transistors. After a brief review of device features and the development of a large-signal simulation model for the SiGe HEMT, the mixer circuit will be discussed in detail.

II. SIGE HEMT TECHNOLOGY

In the SiGe HEMT, a 2DEG forms in a strained Si layer sandwiched between two n-doped SiGe supply layers [7]. In order to form relaxed SiGe layers, a graded buffer is grown on the Si wafer. The gate is formed by a Schottky-type contact. It has a length of 100nm and is centred between the source and drain implant areas which have a spacing of 1μm. The device exhibits n-channel depletion mode behaviour with a threshold voltage of typically V_{th}=-0.7V. Although devices with much higher f_T/f_{max} have been demonstrated [2], the transistors used for model extraction show a maximum f_T of 50GHz and f_{max} of 80GHz (defined via Mason's unilateral gain). Maximum transconductance is 240mS/mm.

III. LARGE-SIGNAL MODEL

The design of mixer circuits requires a large-signal simulation model, which accurately describes the nonlinearities in the devices responsible for the generation of the frequency translating effect. The model of the SiGe HEMT is based on a typical FET equivalent circuit and uses empirical equations to describe the non-linear elements.

The IV model employs the COBRA equation [8] developed at the National University of Ireland, Dublin, to describe the static drain current source I_{DS} (Figure 1). Other non-linear model elements are Schottky-gate

diodes, gate-source- and gate-drain capacitance as well as an I_{ds} current correction source accounting for low-frequency dispersion effects.

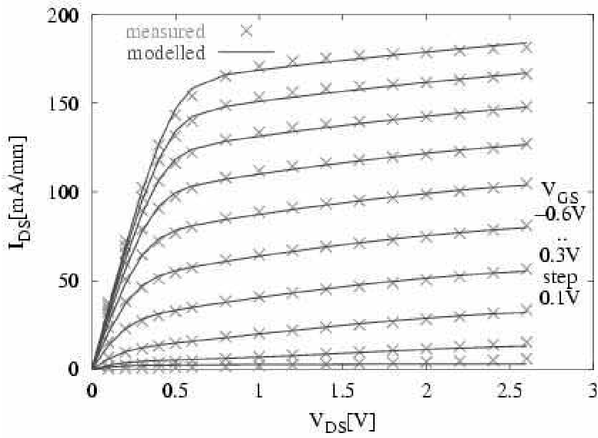

Figure 1: DC-IV model verification of a 0.1µm gate length, 2x50µm width SiGe HEMT transistor.

The dynamic device model is based on analytical extraction of the small-signal model parameters at bias points over the whole IV plane [9] [10]. Figure 2 shows the hereby obtained voltage dependence of C_{gs} and C_{gd}. Empirical expressions are employed to model the non-linear gate capacitances.

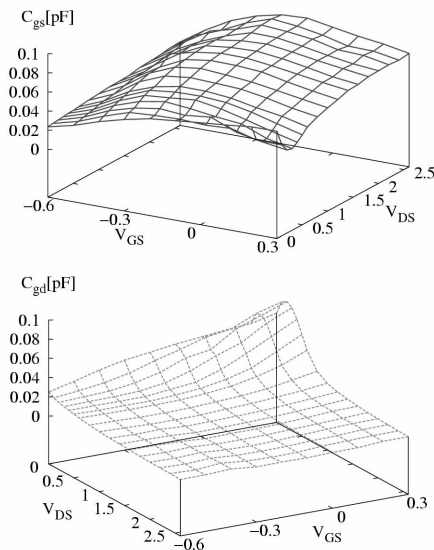

Figure 2 : Gate-Source (a) and Gate-Drain (b) capacitance. Each grid intersection represents an extraction point

LF dispersion effects play an important role in these devices, introducing frequency dependence to trans- and output conductance, and need to be included in the model in order to predict high-frequency behaviour. The dynamic large-signal I_{ds} characteristic is obtained through simultaneous optimisation of the device's trans- and output conductance extracted at high frequencies.

The model is implemented in the ADS simulation environment and can be verified against S-parameter measurements (Figure 3). It is suitable for all types of simulations, ranging from small-signal to full large-signal analyses in the time- and frequency domain.

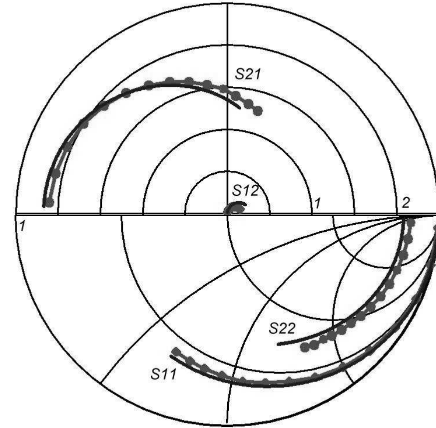

Figure 3 : Comparison of measured and modelled S-parameters up to 40GHz for a typical bias point in saturation. Dotted lines are measured values .The simulation employs the complete large-signal FET model.

IV. MIXER CIRCUIT

The presented mixer circuit uses a single-balanced Gilbert cell topology, with the differential LO signal being applied to the upper transistors of a differential stage (Figure 4), which act as current switches. The lower transistor acts as a common-source amplifier to the RF signal.

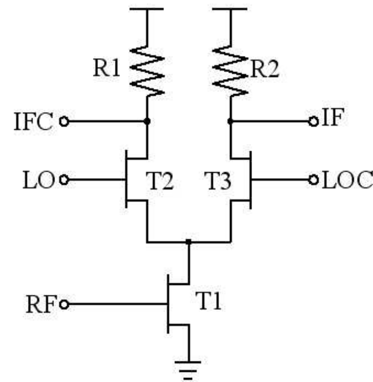

Figure 4 : Schematic of the single-balanced active mixer circuit realized in SiGe HFET technology

The design does not use any frequency selective sections like matching or pole-compensating elements, which results in poor input and output match. However, it allows for the operation of the mixer over a wide range of RF frequencies. Load resistors are chosen to be 200Ω. The presented circuit uses a single metal layer process which excludes the possibility of realizing crossovers as well as MIM capacitors. Due to this technological limitation, several restrictions are imposed on the mixer circuit:

First, the circuit topology cannot exceed a certain level of complexity. For instance, only a half Gilbert cell can be realized to avoid crossovers. Also, the differential LO signal is generated off-chip due to the lack of capacitors.
Second, transistors whose source is not connected to ground can only be realized with a single gate finger in order to eliminate the need for interconnection of transistor source terminals. This imposes a restriction on the total gate width in order to maintain high process yield. Also, it decreases the device's high-frequency performance due to increased gate series resistance. As a compromise with gain and linearity considerations, 100µm gate width transistors have been employed in the present design. Figure 5 shows the layout of the mixer. A redundancy for choosing the drain load resistors is contained. The IC is designed for on-wafer measurement and employs coplanar probe pads with 100µm pitch. Chip dimensions are pad-limited with a total size of 700µm x 560µm.

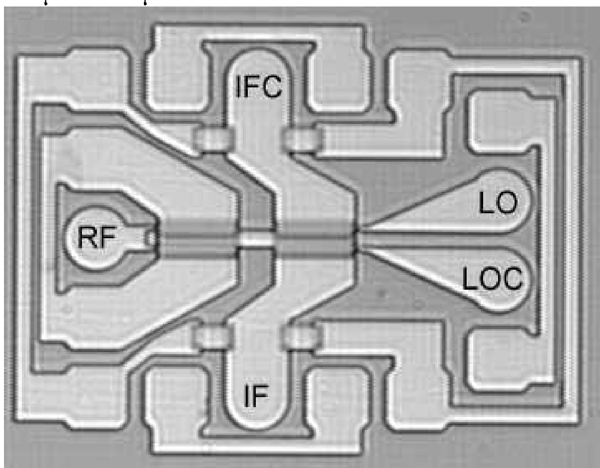

Figure 5: Microphotograph of the SiGe HFET mixer MMIC

For the merit of a simple circuit topology, the differential stage was not de-coupled from the 50Ω measurement environment via source follower stages. Therefore, the load impedance seen by the differential stage is the DC load resistor in parallel with 50Ω. Simulations indicate that conversion gain could be boosted significantly if source follower stages were included to increase the load impedance.
More complex mixer prototypes making use of a second metallization layer are currently being processed. They will include source follower- as well as on-chip single-ended to differential conversion stages.

V. EXPERIMENTAL RESULTS

The frequency translating measurement is performed with the Rohde&Schwarz ZVK vector network analyzer. Cable losses are taken into account and all power levels are corrected to the probe-tip reference plane. The differential LO signals are generated via an external BALUN which adds an additional 1dB loss to the applied LO power. Intermediate frequency power is measured single-ended, with the second output port (IFC) being terminated by a 50Ω impedance. As a consequence, 3dB need to be added to the measured conversion gain to describe the differential situation.
Bias conditions are 5V supply voltage, a V_{GS} of -0.2V for maximum transconductance of the amplifying transistor and 1.2V gate voltage for the switching transistors.
At DC, the realized devices show an increased parasitic contact resistance of the drain and source implant areas, while above some corner frequency, the device characteristics take on their initial values. As a result, effective gate-source bias voltages of the transistors are reduced, leading to an onset of conversion gain saturation at lower LO power levels, but also to a reduction in gain. The model accounts for this effect by parallel R-C networks at the drain and source terminals of the device. The values of the increased DC contact resistance and the bypassing capacitance can be extracted from DC-IV and gain versus frequency (S_{21}) characteristics.
Conversion gain is found to be -4.0dB and -4.7dB when down-converting 3.0GHz and 6.0GHz RF signals, respectively, to an intermediate frequency of 500MHz using high-side injection of an LO power of 5dBm (Figure 6). Simulation accurately predicted the conversion gain for all LO power levels, including the linear amplification region, the "knee" region where the LO transistors start acting as switches as well as the saturated switching regime.

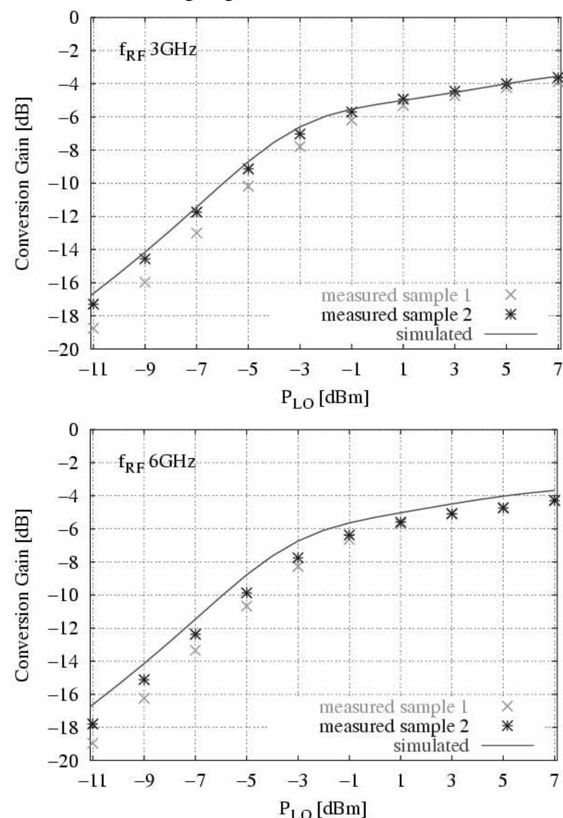

Figure 6: Conversion Gain versus LO power for down-conversion of 3.0GHz (above) and 6.0GHz (below) signals to 500MHz IF. RF power is -20dBm.

Sweeping the applied RF power at f_{RF}=6GHz yields an input related 1dB compression point of -8.8dBm (Figure 7). Table 1 summarizes the measured and simulated results.

f_{RF}	Measurement	Simulation
3GHz	-9.5dBm	-10.0dBm
6GHz	-8.8dBm	-10.8dBm

Table 1: Measured and simulated 1dB compression points (input related)

The mixer exhibits less than 8dB conversion loss for RF frequencies up to 10GHz (Figure 8).

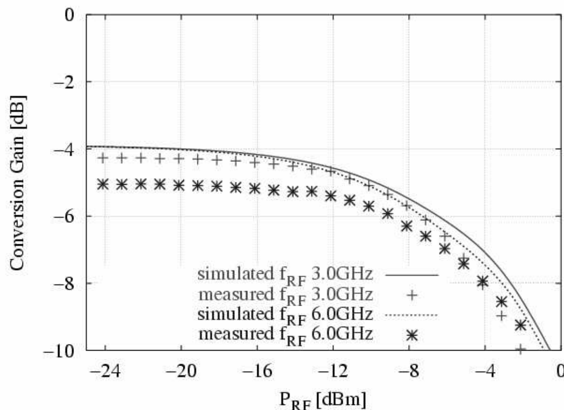

Figure 7: Conversion Gain versus RF power. IF 500MH00z, LO power 5dBm (HSI).

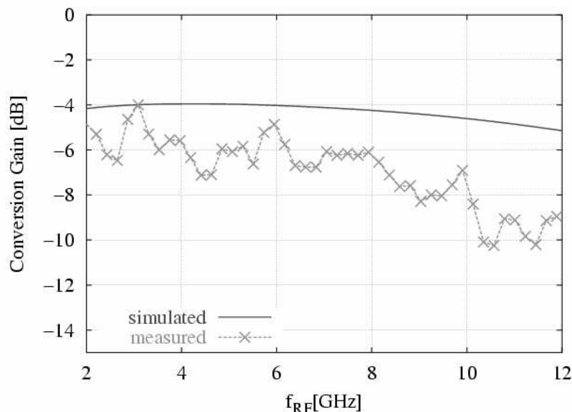

Figure 8: Conversion Gain versus RF frequency for down-conversion to 500MHz IF.LO power is 5dBm (HSI).

VI. CONCLUSION

On the basis of a new large-signal simulation model, the first SiGe HEMT active mixer IC has successfully been designed, processed and characterized. In good agreement with simulation predictions, the mixer exhibits a conversion loss of 4.0dB for down-conversion of a 3.0GHz RF signal to an intermediate frequency of 500MHz. At 6GHz RF, conversion loss is 4.7dB. These results, obtained from the first manufactured wafers and the high model quality are encouraging for the design of more sophisticated mixer structures like e.g. double-balanced Gilbert cells including source follower stages. Further improvement is expected from the inclusion of matching networks for operation at specific frequencies.

ACKNOWLEDGEMENT

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