RF POWER PERFORMANCE OF PASSIVATED ALGAN/GAN HFETS GROWN ON SIC AND SAPPHIRE

H. Leier, A. Wieszt, R. Behtash, H. Tobler, A. Vescan, R. Dietrich, A. Schurr,
H. Sledzik*, JCH. Birbeck, RS. Balmer** and T. Martin****

DaimlerChrysler AG, Research and Technology, P. O. Box 2360, D-89013 Ulm, Germany
phone:+49-731-505-2030 / fax: +49-731-505-4101 / e-mail: helmut.leier@daimlerchrysler.com
$^{+}$ *EADS Deutschland GmbH, Systems & Defence Electronics, Woerthstrasse 85, D-89077 Ulm, Germany*
$^{++}$ *QinetiQ Malvern,Worcs WR 14 , 3PS, United Kingdom*

ABSTRACT

We have analysed the impact of SiN surface passivation on the performance of undoped (piezo) AlGaN/GaN HFETs grown on SiC and sapphire. Though there is little change after passivation in carrier concentration and mobility as evidenced by Hall measurements the RF power performance is significantly improved leading to state of the art power densities of up to 6.5 Watt/mm at 10GHz and absolute power of 6.6 Watt cw for a 1.2mm piezo device on SiC substrate.

INTRODUCTION

GaN/AlGaN HFETs have attached considerable interest in the last few years for power applications at high frequencies. The considerable effort stems from the unique material properties of the III-Nitride semiconductors leading to high breakdown fields in conjunction with good electron transport properties. The GaN/AlGaN HFET technology offers especially large potential to surpass existing device limitations in RF output power, operation voltage and operation temperature at frequencies up to X-band and even above. Indeed impressive high frequency results have been reported recently for GaN/AlGaN HFETs with record power densities of up to 9.8 Watt/mm measured at 8 GHz by Wu et al (1).
In this paper we discuss our recent results on passivated piezo GaN/AlGaN HFETs grown on SI SiC and sapphire by MOCVD. It is shown that the socalled "current compression" effect could be significantly reduced for both device structures using a thin SiN passivation layer.

TECHNOLOGY

The wafers were grown by MOVPE using a Thomas Swan Close Coupled Showerhead reactor. Trimethyl Gallium and Trimethyl Aluminium were used as the group III precursors and the growth was monitored in real time by spectral reflectrometry (300-750nm).

Two piezo wafers were grown with nominally the same vertical structure: one wafer on semi-insulating SiC substrate (wafer A) and one wafer on sapphire substrate (wafer B). A typical HFET structure consists of a nucleation layer, a 1 µm thick GaN buffer layer and an undoped 28nm thick AlGaN layer with Al content of 24-26%.

The device fabrication was performed using mesa isolation with BCl3/Ar gas, ohmic metallisation with Ti/Al/Ni/Au annealed at 900°C for 30 seconds and formation of a T-shaped e-beam gate (Ti/Au) with 0.45µm gate-length. Then a 200nm thick PECVD SiN deposition at 300°C followed. CF4/O2-RIE was used to open contact holes in the SiN layer. Finally Au air-bridges with 2.5µm thickness were fabricated to connect the source pads of multi-finger devices. TLM analysis shows for both wafers contact resistances of 0.5Ohm x mm and sheet resistances between 500 and 600 Ohm/sq.

DC PERFORMANCE

The Hall sheet concentrations and mobilities received from wafer A and B are nearly identical and within the experimental uncertainty unaffected by SiN passivation. This behaviour is consistent with recently published results [2]. The corresponding values for both wafers are:

- Wafer A: ns=1.1x1013/cm^2 , mobility of 1100cm2/Vs
- Wafer B: ns=1.0x1013/cm^2, mobility of 1170cm2/Vs.

The I-V characteristics, however, reveal a significantly lower Idss for the devices grown on sapphire compared to SiC. The passivated (unpassivated) drain currents at Vgs=0V for small area devices on wafer B correspond to 680mA/mm (630mA/mm) whereas the same devices on wafer A exhibit values of 1250mA (1150mA). Also the maximum transconductance of unpassivated devices on wafer A are about 30% higher compared to the corresponding devices on wafer B (220mS/mm compared to 170mS/mm). After passivation a slight increase of about 10% in gm is observed which correspond to recent results on doped AlGaN/GaN HFETs [2,3]. The relative large difference in Idss could be partly explained by the better heatspreading and heat removal for devices on SiC. Indeed, pulsed I-V measurements performed on devices of wafer B show an increase of Idss of up to 880mA/mm.

The observed increase of Idss in our experiments after SiN deposition could obviously not be explained by an increase of ns. Also we found that the threshold voltage didn't change significantly (<0.1Volt) after passivation in good agreement with the constant ns from the Hall measurements. However, the results could be understood in terms of a change of the effective gate-length due to passivation. Assuming charged surface states in the gate-drain region of the AlGaN/GaN HFET without SiN passivation an enhancement of the lateral gate-drain depletion region will occur, resulting in a longer effective gate-length, hence lower maximum transconductance and saturation current. The SiN layer compensate charged surface states, leading to a reduced effective gate length as discussed by Lee et al (2). A comparison of the small signal equivalent circuit parameters of unpassivated and passivated devices carried out by Lee et al (3) reveals a decrease of the transist time for passivated devices consistent with the above speculation.

RF POWER PERFORMANCE

RF power measurements have been performed at 2GHz and 10GHz. At 2GHz a load-pull setup with ATN tuners have been used. It should be mentioned that for this setup the load conditions could not be fully optimized for the smaller devices due to the setup limits and larger devices could not be driven in compression due to a limited power source at 2GHz. At 10GHz the measurement system is based on a Wiltron Model 360B Vector Network Analyser with a Model 3636A test set. For load tuning an active load tuner is applied with up to 20 Watt power handling in the frequency range of 8GHz to 18GHz. As reference, a part of our devices have been measured at Agilent, Santa Clara. All power results presented have been achieved by biasing the devices at class AB. Due to self-biasing the current typically increases during a power measurement.

The impact of SiN passivation on the RF power performance have been studied first at 2GHz. HFET devices with 2x100µm gate width have been selected for this comparison. Fig.1 depicts Pout, gain and PAE versus Pin for a passivated and an unpassivated device of wafer B (sapphire) at Vds=25 Volt and Vgs=-3.8Volt. The unpassivated device delivers 1.7W/mm saturated output power density and the passivated device shows an improved power density of 3.1Watt/mm. The corresponding maximum PAE increases from 41% before passivation to 55% after passivation. From the load impedance Z_L ,which was the same for passivated and unpassivated devices one can estimate the current and the voltage swing. We obtain 490mA/mm and 660A/mm for the unpassivated and passivated devices, respectively, demonstrating that the reduced output power for unpassivated devices is due to a limited RF current drive. In contrast, for passivated devices the calculated current swing is very close to Idss (see above) corresponding to a large reduction of the current compression effect.

Higher absolute output powers and power densities have been achieved at larger drain bias. At Vds=35V a Pout of 28.7dBm corresponding to 3.7Watt/mm with an associated gain of 11dB and a PAE of 40% is obtained.

As expected we observe only a slight decrease of the linear power gain which is probably due to the increased Cgd after passivation (see Fig.1). The observed large increase of power densities after passivation have been seen on all measured devices of wafer B (22 devices measured).

Fig. 2 shows the corresponding comparison of unpassivated and passivated 2x100µm devices on wafer A (SiC). Similiar as for the devices on wafer B a strong increase in Pout and PAE is observed after passivation. At the bias point of Vds=25Volt and Vgs=-4.5Volt the RF power is increased from 24.8dBm to 29.1 dBm and the PAE increases from 35% to 59%. The highest output power on the passivated 2x100µm devices have been measured at Vds=40Volt with Pout=30.9dBm (6.1Watt/mm) and PAE=42%.

Load-pull measurements at 10GHz have been performed on passivated devices on wafer A (SiC). Fig. 3 depicts the output power, PAE and gain of a 4x50µm device biased at Vds=45 Volt. We achieve a power density of 6.5Watt/mm with an associated PAE of 42%. The highest absolute cw output power have been achieved on a 1.2mm device (8x150µm) at Vds=37Volt (Fig.4) with Pout=6.6Watt and a corresponding PAE of 46%.

CONCLUSION

The impact of SiN passivation on (piezo) AlGaN/GaN HFET devices grown on SiC and on sapphire substrate have been reported. We demonstrate that the RF power performance is dramatically enhanced by deposition of a thin SiN film for devices on sapphire as well as on SiC. Maximum output power levels of 6.6 Watt cw and 6.5Watt/mm at 10 GHz have been achieved. We observe little change after passivation in carrier concentration and mobility as evidenced by Hall measurements. Our results are consistent with the assumption that during RF drive the surface of the unpassivated device (e.g. between gate and drain) is negatively charged depleting the channel and thus limiting the RF current amplitude.

ACKNOWLEDGEMENT

The authors wish to acknowledge the support by Alex Cognata from Agilent, Santa Clara for his RF power measurement expertise and measurements done on our devices. The Qinetiq contribution to this work was undertaken as part of Technology Group 7 of the UK MoD Corporate Research Programme.

REFERENCES

(1) Y.-F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, U.K. Mishra
Very-High Power Density AlGaN/GaN HEMTs
IEEE Trans. Electron. Dev., Vol. 48, No. 3, 2001

(2) J-S.Lee, A. Vescan, A. Wieszt, R. Dietrich, H. Leier, Y-S.Kwon
Characteristics of AlGaN/GaN HEMT Devices with SiN Passivation
IEDM 2000, Conference proceedings

(3) J-S.Lee, A. Vescan, A. Wieszt, R. Dietrich, H. Leier, Y-S.Kwon
Small signal and power measurements of AlGaN/GaN HEMT with SiN passivation
Electron. Lett, vol 37, no.2, 130-132

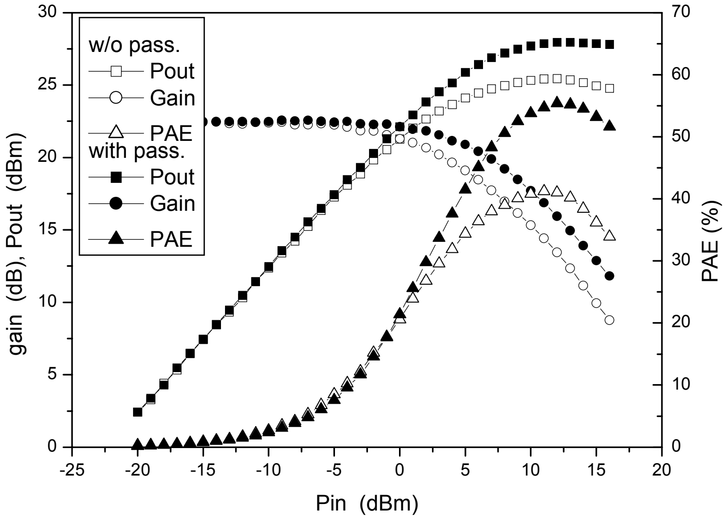

Fig.1: Power sweep at 2GHz before and after SiN passivation (Wafer B, sapphire substrate)

Fig.2: Power sweep at 2GHz before and after SiN passivation (Wafer A, SiC substrate, 2x100µm, Vds=25Volt)

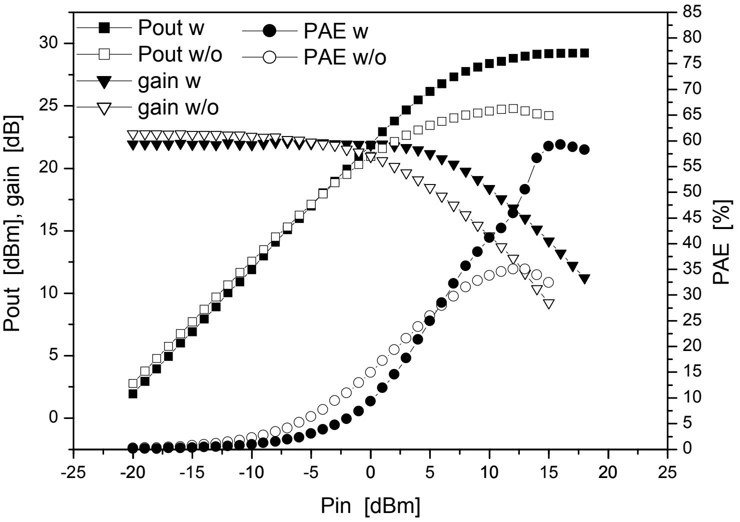

Fig.3: Power sweep at 10GHz after SiN passivation (Wafer A, SiC substrate, 4x50µm, Vds=45Volt)

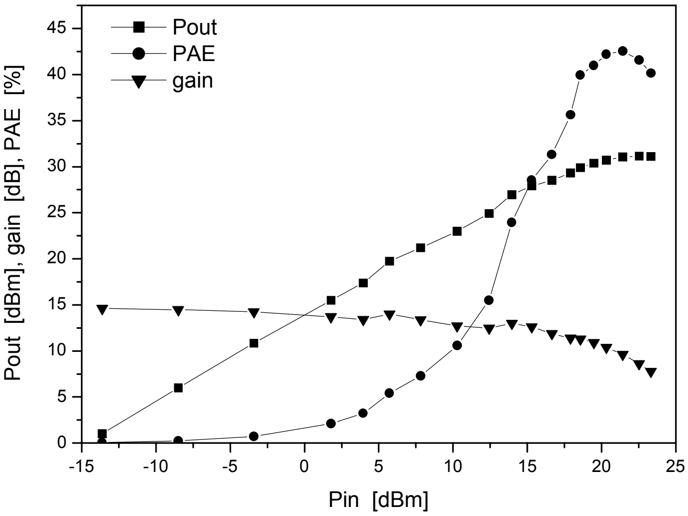

Fig.4: Power sweep at 10GHz after SiN passivation (Wafer A, SiC substrate, 8x125µm , Vds=37Volt