0.12 µm GATE LENGTH $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HEMTs ON TRANSFERRED SUBSTRATE

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ABSTRACT

New $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ transferred-substrate high electron mobility transistors (TS-HEMTs) have been successfully fabricated on 2 inch Silicon substrate with 0.12 µm T-shaped gate length. These new TS-HEMTs exhibit typical drain currents of 450 mA/mm and extrinsic transconductance up to 770 mS/mm. An extrinsic current cutoff frequency f_T of 185 GHz is obtained. That result is the first reported for $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ TS-HEMTs on Silicon substrate.

INTRODUCTION

In the recent few years, High Electron Mobility Transistors (HEMTs) with nanometer gate length are of interest particularly for high-speed optical communication system. InP-based InAlAs/InGaAs HEMTs have the potential to achieve high maximum oscillation frequency f_{max}. A value of 600GHz has been achieved with a 0.1 µm gate length LM-HEMT on InP [1]. In sub-0.1 µm gate length device, short-channel effect will be a limiting factor in the improvement of f_{max}. Indeed injection of carriers in the substrate, when shorting gate length, will drastically degrade the output conductance gd of the device. The way to suppress injection of these carriers is to replace the substrate by an insulating layer. This can be achieved by a transferred-substrate technique previously used in SOI-MOS and TS-HBT [2] technologies.
In this paper, we demonstrate the feasibility of the first transferred-substrate HEMT (TS-HEMT) technology process. DC and RF performance of this new device are reported.

MATERIAL GROWTH AND DEVICE FABRICATION

Figure 1 shows the schematic cross section the InAlAs/InGaAs/InP structure transferred on the Silicon substrate. InAlAs/InGaAs/InP HEMTs structure and Silicon wafer were bonded by means of SiO_2-SiO_2 bonding [3,4].
Lattice-matched InAlAs/InGaAs layers were grown on 2-inch InP substrate by Molecular Beam Epitaxy. In comparison to typical structure used for conventional lattice-matched HEMTs on InP substrate, the heterostructure has been reverse grown. First a 0.4 µm thick etch-stop layer of InGaAs was grown and was followed by a 100 Å InAlAs layer. These layers are essential to the etching of the InP substrate. Then the reverse FET structure growing was begun. It consists on a

100 Å n+ InGaAs cap layer, a 120 Å undoped InAlAs Schottky contact layer, a Silicon delta-doping plane, a 50 Å undoped InAlAs spacer and the 200 Å undoped InGaAs channel. This was following by a 0.3µm InAlAs buffer layer. Lastly a 200 Å InP layer was realized to reduce surface oxidation. The main difficulty associated with the growth of the reverse heterostructure is the Silicon segregation from the cap layer in the Schottky contact layer and more from the delta-doping plane in the channel layer which drastically reduces the electron mobility. These have been overcome by choosing a suitable growth temperature sequence.

The InP wafer with its heterostructure was bonded onto a 2-inch FZ silicon wafer at room temperature by means of SiO_2-SiO_2 bonding. For this, the two substrates were covered with a layer of PECVD SiO_2. Before bonding, both wafers were polished to ensure a low roughness and then cleaned. The bonded wafers were annealed at 200°C for 60 min to increase the bonding energy. The total thickness of the SiO_2 film between the heterostructure and Silicon substrate is ~ 550 nm. The infrared transmission image of the bonded InP/Si wafers shows a good quality bonding on the full wafer (Figure 2).

To uncover the cap layer, etch-stop layers were removed by wet chemical etching (figure 1). The InP substrate was removal by Hydrochloric solution. The InGaAs layer was selectively etched by Succinic Acid, ammonia and hydrogen peroxide solution. The 100 Å InAlAs layer is then removed by low etching rate H_3PO_4:H_2O_2:H_2O solution.

Then the 0.12 µm T-shaped gate length HEMT fabrication can be started. It is exactly the same process used on classical LM-HEMTs. First, the mesa was defined by wet chemical etching using H_3PO_4:H_2O_2:H_2O solution. To form ohmic contacts, Ni/Ge/Au/Ni/Au metalization was evaporated and followed by rapid thermal annealing at 310°C for 60 seconds. TLM measurements show a typical ohmic contact resistance of about 0.25 Ω.mm, with a root mean square of 0.05 Ω.mm. The T-shaped gates were defined by electron beam lithography using a bilayer PMMA/(PMMA-MAA) resist scheme. The gate length L_g was 0.12 µm. Selective gate recess etching was performed using a solution of Succinic Acid (SA), ammonia and hydrogen peroxide. The gate metalization was Ti/Pt/Au. Lastly thick Ti/Au layers were evaporated to form bonding pads.

DC AND MICROWAVE CHARACTERISTICS

DC and microwave characteristics of 100 µm wide TS-HEMTs were measured on wafer. The I(V) characteristics are given in figure 3. The device exhibits drain-to-source current I_{ds} = 450 mA/mm at gate-to-source voltage V_{gs} = 0.4 V and drain-to-source voltage V_{ds} = 1 V. The pinch-off voltage V_p is –0.6 V. The maximum extrinsic transconductance gm is 770mS/mm at V_{ds} = 1 V and V_{gs} = -0.25 V.

Using S-parameters measurement in the 0-50GHz frequency range, calculated extrinsic current gain $|h_{21}|^2$ and maximum stable gain MSG are plotted in figure 4 versus frequency. On the same graph, stability factor k is also given. Extrapolation by 20 dB/decade of $|h_{21}|^2$ gives an extrinsic cutoff frequency f_T of 185 GHz. This result is close to published results obtained with LM-HEMT on InP [5]. Maximum oscillation frequency f_{max} deduced from extrapolation by 20 dB/decade of MSG is 290 GHz. This evidences the growth quality of the reverse heterostructure and shows that the transferred-substrate process affects very weakly the microwave performances of the TS-HEMTs.

CONCLUSION

Transferred-substrate InAlAs/InGaAs 0.12 µm T-gate length HEMTs on Silicon substrate have been successfully fabricated, and demonstrates the feasibility of such device. Typical drain-to-source current I_{ds} of 450 mA/mm and extrinsic transconductance gm of 770 mS/mm were obtained with our devices. Current gain cutoff frequency f_T = 185 GHz is achieved and is comparable to reported data of LM-HEMT on InP. Although the InAlAs buffer has not been removed, f_{max} reaches 290GHz. By removing this layer, improvement of fmax is expected. This new device will be investigated in the near future.

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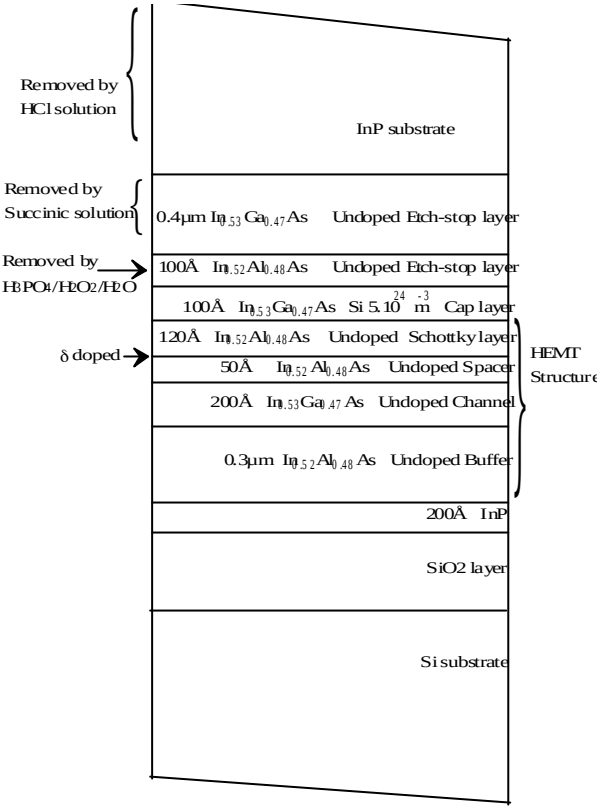

Figure 1: Schematic cross section of the reverse $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HEMTs structure on InP substrate reported on Silicon substrate. The delta-doped Silicon density is 5.10^{12} cm^{-2}.

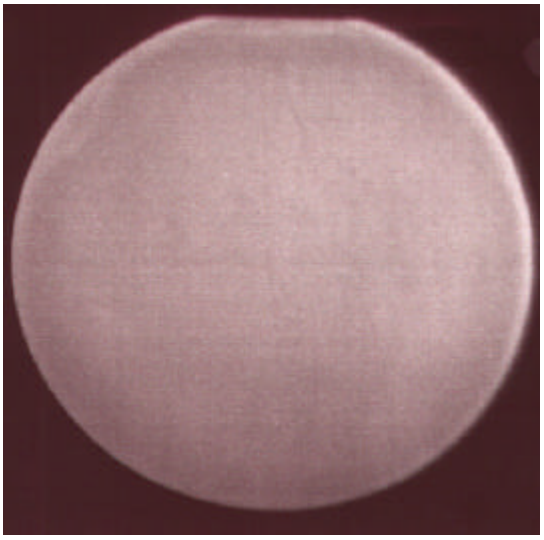

Figure 2: IR transmission image of InP wafer with its heterostructure bonded onto Si wafer (2 inch diameter), annealed at 200°C

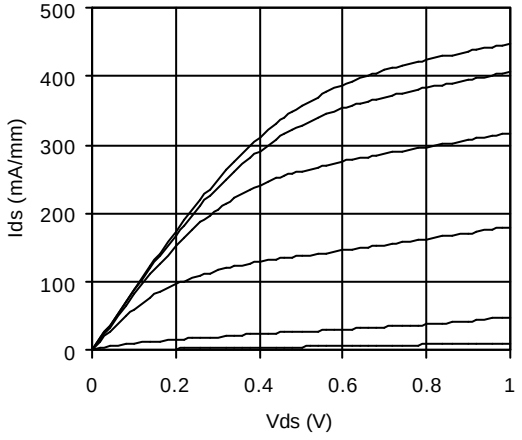

Figure 3: I(V) characteristics for a 0.12x100 µm² TS-HEMT. The pinch-off voltage V_p is -0.6 V. The gate step voltage is 0.2V.

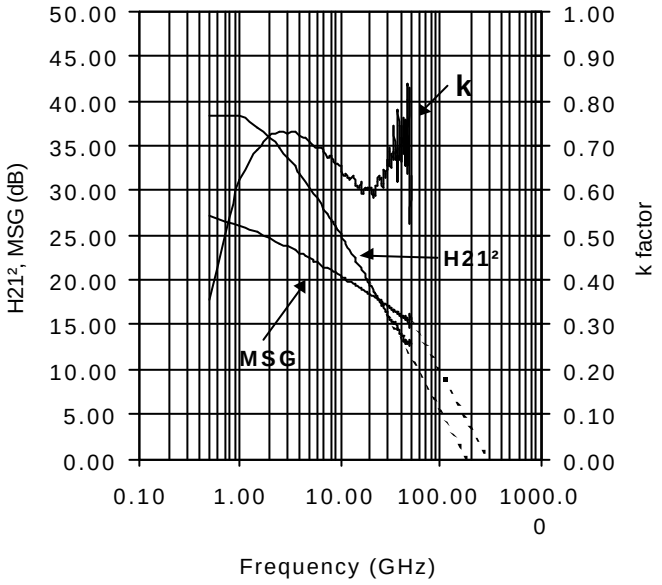

Figure 4: Extrinsic current gain $|h21|^2$ and maximum stable gain MSG versus frequency. The drain-to-source voltage V_{ds} is 1 V and the gate-to-source voltage V_{gs} is –0.25 V. On the same graph, the stability factor k is also plotted.