Electro-Thermal Modelling of Very High Power Microwave Bipolar Junction Transistors

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***Abstract* — This paper describes a new approach to accurately characterise very high power, Si BJT, devices capable of delivering powers in excess of 250W, at L band, in a class C amplifier configuration. Conventional modelling approaches are not suitable for large power structures. An alternative electro-thermal, equivalent circuit model, has been constructed using a novel hierarchical approach. The thermal dependence of the device characterisation is removed during the extraction of the electrical circuit and is reinserted, within the model, using a suitably complex thermal network, determined using a fully physical thermal simulator. Theoretical and experimental results are shown for steady state and pulsed amplifier operation.**

I. INTRODUCTION

The Si BJTs considered in this work remain some of the most suitable devices for very high power applications at low microwave frequencies. The modelling of small-scale microwave devices is typically based on either a fully physical simulation or an equivalent circuit approach. For large power structures a fully physical model generally requires intolerable computational resources and the equivalent circuits documented generally fail to address issues specific to large power structures.

II. ELECTO-THERMAL MODELLING APPROACH

The hierarchical approach adopted in this work is central to the modelling of the complex electro-thermal interaction that governs large power device operation. During the electrical characterisation thermal effects are removed and scaling is applied to deconstruct the large power device into an array of elementary structures, each modelled using a separate intrinsic device model. Each sub-element's temperature dependence is characterised using traditional SPICE equations with the temperature of each elementary unit, and the complex thermal interaction between all units, modelled using a detailed thermal resistance matrix. The non-uniform behaviour of the device can be re-injected into the complete model by solving the electrical and thermal circuits consistently within conventional simulation software.

A. *Device Hierarchy*

Because of measurement difficulties, PA designers are often forced to characterise smaller devices and apply suitable scaling, effectively constructing the power device from its constituent elements. This situation is undesirable, since the entire device will be influenced by secondary effects not accounted for during the linear scaling process. The dominant secondary effect, preventing the linear scaling of measured data, is typically the non-uniform thermal distribution exhibited within a power device.

A pulsed I-V measurement system can be used to extract isothermal DC data, McIntosh et al (1). Self-heating will be avoided providing the pulse width used is significantly smaller than the thermal time constant of the device. The measured data can be used to extract DC parameters for the Gummel-Poon model, Hafizi et al (2). Since this data corresponds to a uniform device temperature, the extracted model parameters can be accurately scaled linearly to reduce the power device to a series of smaller sub-structures each modelled using a separate intrinsic device model. The thermal interaction between these sub-structures is characterised by a thermal equivalent circuit, compatible with the level of deconstruction adopted and determined using a tailored, fully physical, thermal simulation.

The technique described is flexible in that it allows a large device to be broken down into a series of smaller structures. The degree of deconstruction is based on the lowest level heat source assumed and will determine the accuracy of the model. Strictly speaking each emitter finger within every device cell represents a heat source and so should be modelled using a separate intrinsic model with an individual temperature. However compromises can be made, to reduce the complexity and computational resources required by the model. A device cell, or even an entire die, may exhibit an approximately uniform temperature profile allowing such elementary structures to be represented by a single intrinsic device model.

B. Device Parasitics

The extraction of parasitic element values based on simplified extrinsic network topologies has been well documented for FETs and modified for HEMT and HBT structures. In a large power device, containing internal matching circuitry, such extrinsic circuits typically fail to provide adequate representation. Based on structural considerations it is often possible to identify the dominant parasitics that exist at each level of the device hierarchy (Figure 1). It may also be possible to estimate some of these element values using physical approximations so as to reduce the extent of the extraction procedure.

By performing a pulsed s-parameter measurement on a pulsed DC bias, self-heating can be eliminated from the s-parameter data. The identified parasitic elements can be grouped and extracted based on measurements taken under 'cutoff' and 'saturation' bias conditions, Gobert et al (3). Based on similar arguments to those already discussed the extrinsic element values can then be linearly scaled based on the level of device deconstruction adopted (Figure 2).

C. Thermal Considerations

Thermal equivalent circuits have been presented for multiple finger structure devices. The model topology proposed by Snowden (4) has been considered in this work because of its generality. This model acts as a framework for a detailed fully physical thermal simulation. Once constructed the thermal solution reduces to simple matrix multiplications making the complete electro-thermal model suitable for CAD applications.

A generalised rectangular block of semiconductor material with known thermal conductivity, $k(T)$, is considered. The steady state heat diffusion equation represents a non linear partial differential equation as a result of the temperature dependence of thermal conductivity and is difficult to solve. Based on the Kirchoff transformation, Joyce (5), a linearised heat diffusion equation can be defined which can then be solved subject to given boundary conditions. The boundary conditions used are based on the assumptions that the top surface has a specified power distribution, the bottom surface is at a constant temperature and all other surfaces are adiabatic.

A versatile thermal simulator based on a surface approximation of the solution to the 3-D heat flow equation, Liou (6), has been developed. This program calculates the temperature distribution across a large device structure characterised by a number of, arbitrarily aligned, rectangular 'heat sources' and a given power dissipation. The program requires the construction of a surface mesh and implements the double Fourier expansion technique to minimise simulation time. This program can also be used to determine the thermal resistance matrix by consecutively heating each source and calculating the average temperature across all other sources. In keeping with the hierarchical framework the program is flexible enough to allow the thermal resistance matrix to be determined based on the low level temperature source assumed allowing the electrical and thermal equivalent circuits to be derived consistently, based on the overall level of model complexity required (Figure 3).

An improved thermal characterisation can be obtained based on a fully analytical solution to the steady state 3-D heat flow equation, Batty et al (7). This approach allows the inclusion of generalised surface heating elements since heating areas are not required to conform to a surface mesh. Based on this approach a much more efficient, fully analytical, expression for the thermal resistance matrix elements can be defined. This analytical solution can also be extended to multi-layer structures allowing the determination of a more accurate thermal resistance matrix, Batty et al (7).

III. MEASURED PERFORMANCE

The 250W BJT power device modelled in this work has been operated as a class C pulsed power amplifier. Figure 4 shows the test set-up used.

A. *Temperature Measurement & Emissivity Correction*

The set-up was initially used with a de-capped device to investigate the internal temperatures across the multiple die structure under pulsed operating conditions. This required the use of a super cooled thermal camera and a pre-calibration procedure, Webb (8) used to construct an emissivity map of the internal device. The corrected measured results are shown in Figure 5 and show good agreement with the temperatures predicted by the fully physical thermal simulation.

B. *Thermal Resistance Measurement*

The measurement set-up shown in Figure 4 was also used to establish a value for the global thermal resistance, describing the average temperature variation with dissipated power for the entire device structure. This measurement was performed by varying the duty cycle for a set pulsing frequency (Figure 6). The resulting plot produced an approximately linear characteristic with a gradient related to R_{TH}. A value of R_{TH}=0.23 K/W was obtained from this

measurement, very close to that specified by the manufacturer, and coinciding well with the R_{TH} matrix calculated using the thermal simulator.

IV. CONCLUSION

A methodology has been presented for modelling large scale power device structures using a physics based equivalent circuit approach, implemented within a hierarchical framework allowing the device to be modelled and investigated at different levels of complexity. A number of issues associated with large power devices have been addressed. Temperatures and thermal resistance values predicted by the physical thermal simulator show very good agreement with measured results.

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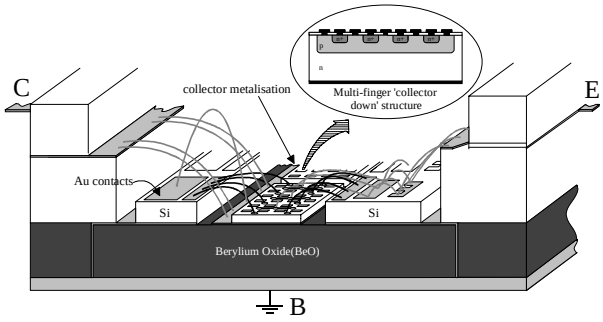

Fig. 1. Complex physical structure of power BJT device.

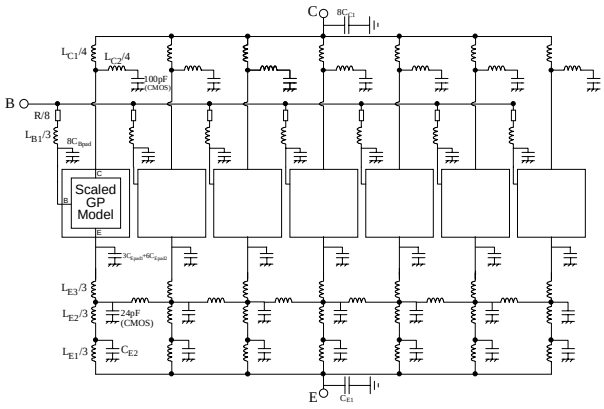

Fig. 2. Example of deconstruction using each die, of a seven die 250W device, as an elementary heat source.

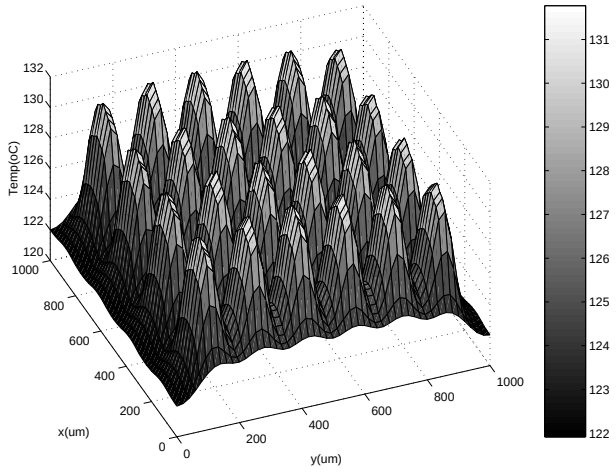

Fig. 3. Simulated thermal distribution across a single isolated die, housing a 6x4 array of transistor devices.

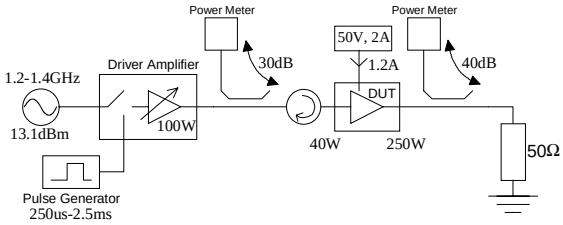

Fig. 4. Measurement set-up used to investigate thermal characteristics associated with pulsed amplifier operation.

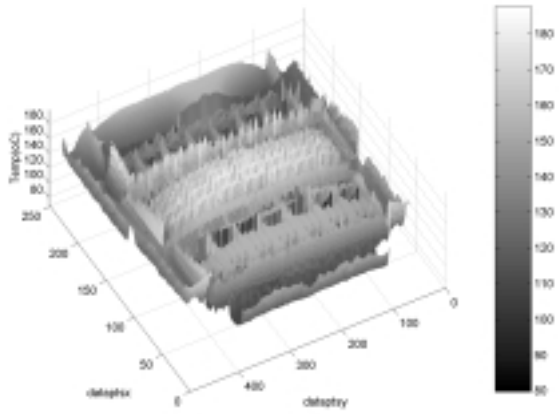

Fig. 5. Emissivity corrected thermal measurement of a power BJT, delivering 250W, in a pulsed class C amplifier configuration.

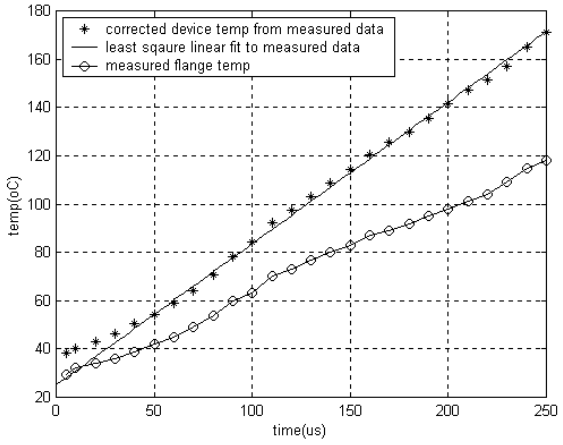

Fig. 6. Measured device temperature variation with pulse width for a fixed pulsing period of 2.5ms.