# Silicon Packaging and RF Solder-free Interconnect for X-band SAR T/R Module

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***Abstract* — This paper presents recent development conducted in the area of RF packaging and interconnect technologies. An original concept of 3D silicon packaging including collective wiring process is proposed and applied to the design of an X-band T/R module demonstrator. An RF solder-less interconnect based on the CIN::APSE connecting system (CINCH™) has been developed to address the need of vertical transition in new generation of SAR active antenna.**

## INTRODUCTION

Two of the most critical challenges of the new generation of X-band SAR instruments will be the performances and the cost of the active antenna. Due to their high number and functional complexity, T/R modules represent a major contributor to these two parameters. Packaging and interconnect technologies have been identified among the main critical issues to be addressed to successfully overcome these challenges.
So, in the frame of a contract founded by the European Space Agency, new developments in these areas have been conducted in close collaboration by Alcatel Space Industries and Thales Systèmes Aéroportés. This study has made profit of advanced packaging technology currently developed at Thales Research & Technology (TRT). This technology is based on two original concepts: collective wiring and silicon substrate. Collective wiring allows the simultaneous wiring of tens of modules as well as their packaging, in a very compact way. The basic idea is to perform the interconnect through mostly photolithographic processes. The dice are first positioned on a substrate and a polymer film is then glued on top. The via holes are laser ablated down to the MMIC pads and the metal interconnect lines between the chips, are realized with a printed circuit board (PCB) like technology. The rationale behind this approach lies in the fact that this technology enables the simultaneous realization of a large number of modules on the same substrate, bringing down the unity cost of a module. The choice of substrate is also an important matter in the overall process as well as performances. High Resistivity (HR) silicon (> 2000 Ω.cm) was chosen for its excellent micro-machinability and its good thermal properties (for dissipating the heat from the MMICs). HR silicon is also a good dielectric material at higher frequencies, as reported by numerous publications.
The solder-less interconnect technologies have known a strong development during the last three years. The advantages of this kind of interconnects (simplification of assembly principle, absorption of mechanical drifts due to thermal coefficient expansion mismatches, easy removal for repair and maintenance, higher integration due to 3D assembly thanks to vertical transition ..) make them very attractive. An RF solder-less connector based on the CIN::APSE interconnect system (CINCH™) has been developed to connect the RF accesses of the T/R module to the radiating panel. This interconnect technology is well suited to the antenna architecture based on a stacking concept.

## SILICON PACKAGING TECHNOLOGY

TRT had already experience in silicon through-hole drilling and collective wiring on silicon substrate. In order to prove the concept, which will be validated through both passive and active demonstrators, different hard points had to be addressed, namely the hermeticity of the package (trough-holes and cover interface) as well as the compatibility of the collective wiring with the sealing process used for the cover.
The choice of the materials (adhesive and dielectric) has been made considering, at first the process compatibility (mechanical constraints, cover sealing, excimer laser and/or plasma ablation, …) and secondly the electrical characteristics ($\varepsilon_r$ and tg $\delta$). Since the cover has to be brazed in order to provide hermetic sealing, various materials which can be used for collective wiring, have been evaluated for compatibility with the brazing process. Different buildups have been tested with a simulation of reflow process (350°C during 1 min). Visual inspection showed no degradation hence the chosen buildup for the demonstrator is the following: Si, thermal oxyde, TiW, Cu (15µm), acrylic resin (thickness: 25 µm, $\varepsilon_r$: 3.6), Arlon (thickness: 47 µm, $\varepsilon_r$: 3,8), Cu (15 µm).
The via holes have been realised for high and low frequency input and output lines. These vias have been realised with localised RIE etch and the oxide layer has been used as a mask. The silicon substrate is 500 µm thick, while the vias have diameter of 200 µm. The vias are etched from the front face. The cavities in which MMIC are positioned, are

realised at same time. The figure shows a top view of via hole (200µm) through the Si substrate with one cavity (1x1 $mm^2$) on each side. Two technologies have been studied for the hermeticity of the via holes (see Fig. 1.c): a *front face process (*via etching, metallisation of front face of substrate, deposition of BCB on front face, BCB etching through photolithography and back face metallisation) and a *back face process (*metallisation of back face of substrate, via RIE etching, localised refill in vias and front face metallisation).
The silicon cover is realised through a RIE etching process over a thickness of 300 µm. The hard solder has been realised with 10µm of Sn/Pb (60/40) deposited over 15µm of Cu (see Fig. 1.a). Brazing of the cover has been done in an infrared conveying oven with these conditions: 260°C to 350°C during 1 min. Shear tests have proved the effectiveness of the sealing process used for the attachment of the cover on the substrate (see Fig. 1.b).

A passive demonstrator (see Fig. 2) was then realized to validate the developed technologies and verify the performances of the RF interconnect (decribed in the next paragraph). It consists mainly of: two RF feedthroughs connected with a 50Ω microstrip line, another RF feedthrough connected to a 50Ω load located on the "50Ω" MMIC and some low frequency inputs/outputs connected two by two. There is also a large size MMIC die included in the demonstrator in order to see the mechanical compatibility of the process with this kind of chip. The passive demonstrator has a size of 2x2 $cm^2$.

The next step is to realise the active demonstrator which consists of a real T/R module. Its layout and a cut view are shown Fig. 3. The receiving channel is composed of 2 Low Noise Amplifier (LNA), 1 attenuator/switch and 1 phase-shifter. The transmitting channel is composed of the phase-shifter, the attenuator/switch, 1 LNA, 1 driver and 1 High Power Amplifier (HPA). The layout also includes the 100pF decoupling capacitors. MMIC and capacitors are glued inside the silicon's cavities by a thermal glue (5W/mK). Receiving and Transmitting channel are isolated from each other by walls of silicon. Because of the large amount of Low Frequency lines, a small opening in the ground plane is realised in order to allow crossing of these lines. To avoid thermal effect, the output CIN::APSE is far from the HPA. The T/R module has a size of 2.7x2.3 $cm^2$.

## SOLDER-FREE INTERCONNECT

To achieve a compact sub-system, the SAR active antenna architecture is based on a stacking concept. Its mechanical structure is sandwiched on one side by the radiating panel (RF multi-layer card) and on the other one by the T/R modules. To connect the RF accesses of the T/R module (silicon package) through the structure to the RF multi-layer circuit a solder-free surface mountable connector (namely CIN::APSE interconnect system) able to provide a vertical transition has been selected.
The principle of CIN::APSE connector is to provide electrical contact between 2 metallic pads thanks to a cylindrical conductor compressed between them [1],[2],[3] (see Fig. 4). For conductor length lower than 0.8 mm the conductor is only made of a button constituted by a very fine gold plated wire randomly distributed into a cylindrical volume. The CIN::APSE button is inserted into an organic carrier (Ultem). The addition on one side of the button of a gold plated brass plunger allows to achieve higher conductor length. In our application the configuration button + plunger has been selected to match with the 3.5 mm thickness structure in which the CIN::APSE interconnect is embedded.

### *A. Interconnect Description*

The objective of this RF interconnect is to steady a waveguide propagation well matched through the CIN::APSE connector from microstrip line on polymer (inside silicon package) to stripline on Duroid substrate (inside RF multi-layer circuit). As regard to the vertical topology of the connection the more appropriate propagation mode inside the CIN::APSE connector is of coaxial type. To generate in CIN::APSE connector a coaxial propagation as close as possible to ideal, an appropriate way is to replace the grounded outer cylindrical conductor of perfect coaxial mode by a crown made of several contacts regularly spaced. Its characteristic impedance depends on the number of contacts and on the crown diameter. The same approach is used in the silicon substrate to propagate a pseudo-coaxial mode thanks to a metal via crown. The overall interconnect has been matched to 50 Ω by optimizing the various internal transitions.

### *B. Interconnect simulated performances*

The full interconnect has been simulated on HFSS (Ansoft ™) which is a 3D E.M. simulator. The overall structure (see Fig. 5) consists basically of a 50 Ω micro-strip line on polymer material (acrylic + Arlon ™), a "coaxial" RF feedthrough in high resistivity silicon substrate, the CIN::APSE connector and a 50 Ω stripline in the lower Duroid substrate.
The number of ground via holes in the silicon substrate and ground contacts of CIN::APSE connector has been reduced to 4 to keep a good rigidity for the substrate and minimize the pressure applied by the CIN::APSE connectors. This reduced number compared to an ideal coaxial transition does not translate into degraded performances. After optimization of the interconnect, the results of the simulations show a low return loss in the frequency band of interest (see Fig. 6).

*C. Interconnect measured performances*

The performances of two cascaded interconnects have been evaluated thanks to a test fixture representative of the T/R module environment (Fig. 7). The active T/R module is replaced by a passive silicon package including only a 50 Ω microstrip line on polymer from the input to one of the output. Test fixture return losses are measured better than -20 dB over the useful frequency bandwidth 9.4 – 9.9 GHz (Fig. 8).

## CONCLUSION

RF packaging and interconnect technologies have been identified as critical issues to be addressed to win the challenges proposed by the new generation of SAR active antenna. New developments in these fields have been jointly conducted by Alcatel Space Industries and Thales Systèmes Aéroportés in the frame of an ESA contract. An original concept of advanced RF silicon packaging including collective wiring has been presented. Recent developments conducted by TRT in the frame of this study aimed to insure package hermeticity as regard to space qualification requirements. Specific effort has been made to process hermetic RF and BF via in silicon substrate and to perform appropriate cover sealing. This technology has been applied to the design of a T/R module demonstrator. An RF solder-free interconnect based on the CIN::APSE connecting system has been designed to address the need for vertical transition due to the stacking architecture of the active radiating panel. Overall interconnect (including CIN::APSE connector and transitions to silicon package and Duroid stripline circuit) simulated return losses are better than –20 dB on a large bandwidth around 10 GHz. A SMA-ended test fixture including 2 cascaded interconnects, a passive T/R module demonstrator and a Duroid stripline circuit presents about -20 dB return losses at 10 GHz which confirms the satisfactory behaviour of the CIN::APSE based interconnect.

## ACKNOWLEDGEMENT

The authors wish to acknowledge Mr Francesc Coromina from ESA for fruitful discussions.

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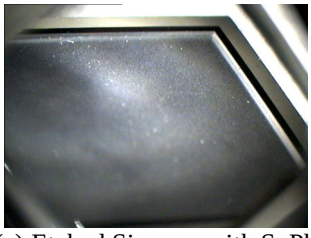
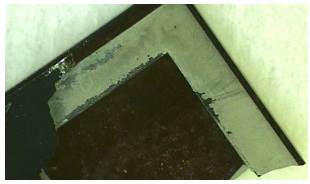
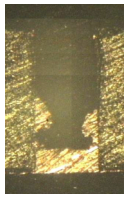


(a):Etched Si cover with SnPb

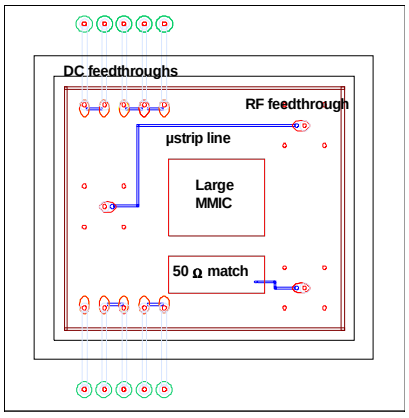


(b): Brazed cover after shear test

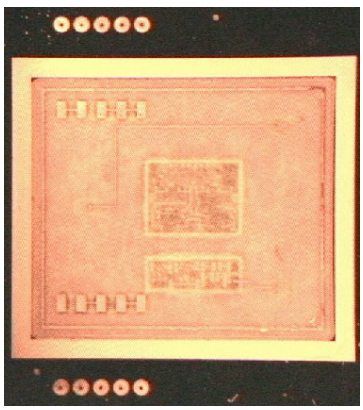


(c): Metal filled via hole

Fig. 1. Silicon packaging



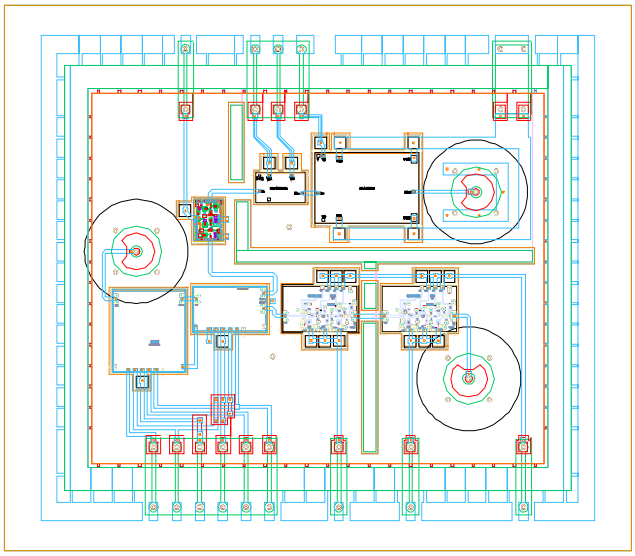

(a): Passive demonstrator layout

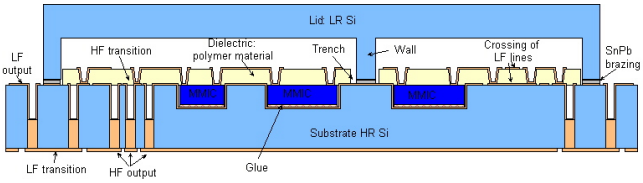


(b): Passive demonstrator

(c): Demonstrator after brazing of the cover

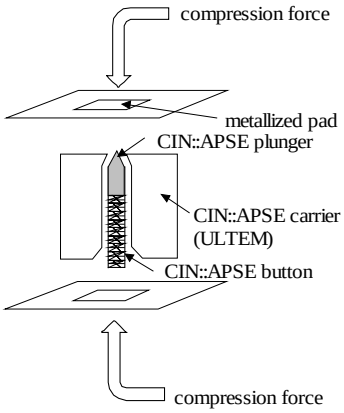
Fig. 2.Passive demonstrator

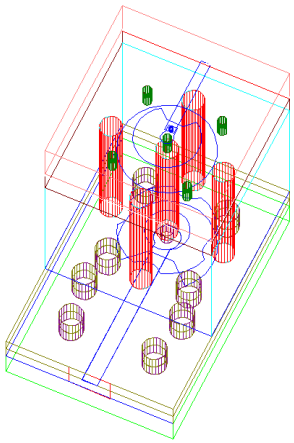





(a): Layout of the active demonstrator (b): Cut view of the active demonstrator

Fig. 3: Active demonstrator layout.



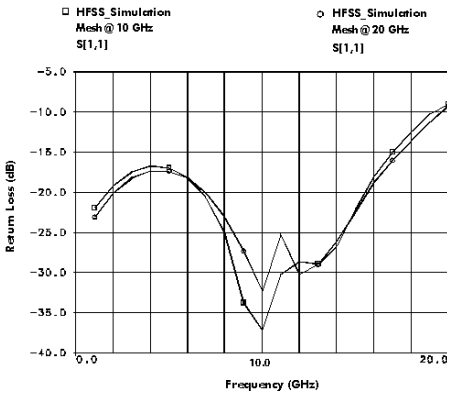
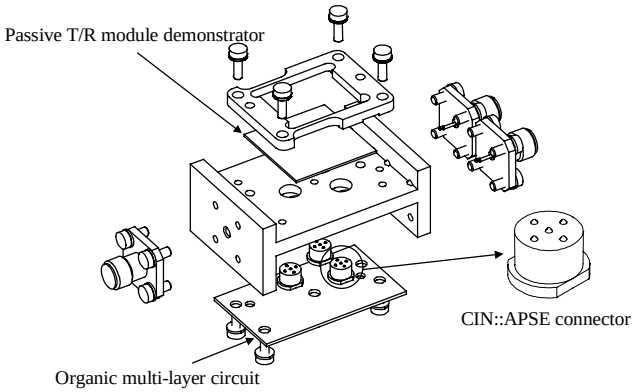



Fig. 4. CIN::APSE contact Fig. 5. 3D layout of the interconnect Fig. 6. Interconnect simulated return losses



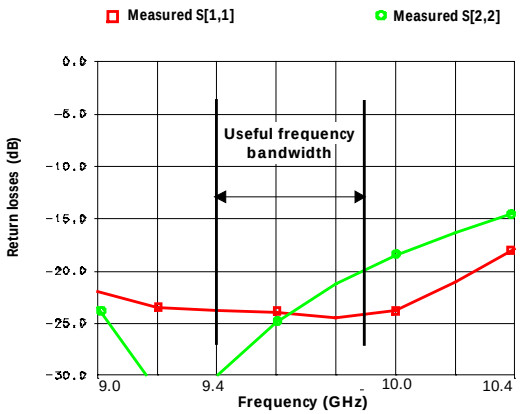




Fig. 7. Interconnect simulated return losses Fig. 8. Test fixture measured return losses