Millimetre-wave Performance of InAlAs/InGaAs HEMTs using a UVIII/PMMA Bilayer for 70nm T-Gate fabrication

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We report the first mm-wave measurements for lattice-matched InP HEMTS with 70 nm T-gates made using a UVIII/PMMA bilayer resist. The measured DC gate resistance was 340 Ω/mm, while the extrapolated f_T of the 70 nm device was ~300 GHz for a 2x50 µm width device.

INTRODUCTION

T shaped gates are commonly used to maximise the high frequency performance of High Electron Mobility Transistors (HEMTs). The performance of transistors incorporating T-gates benefit from ultra short footwidths and large headwidths. The former enhances the high frequency performance while the latter minimises DC and RF losses giving improved high frequency power gain. Record f_T's of 396 GHz have been obtained from 25 nm T-gate HEMT devices [1], whilst a 188 GHz two stage low noise amplifier (LNA) has been fabricated with 9 dB gain using 70 nm InP pseudo-morphic HEMTs [2].

Conventional electron-beam lithography for T-gate fabrication is commonly based on PMMA and related co-polymers. In such resist stacks there is a relatively limited difference in the electron beam sensitivity of the resists and this limits the ultimate cross-sectional dimensions of the T-gates [3]. UVIII is a Shipley DUV photoresist, which is almost five times more sensitive to electron beam exposure than PMMA thus enabling ultra-short footprint T-gates with larger cross sectional areas to be written at higher speeds [4]. The increased cross-sectional area of the gate results in reduced DC and RF resistance/inductance of the gate electrodes giving the highest performance mm-wave devices.

In this paper we report on the first published results of 70 nm T-gate devices made using bilayers of UVIII and PMMA resists.

DEVICE FABRICATION AND PERFORMANCE

The layer structure of the devices used this work were grown in-house by molecular beam epitaxy (MBE) on a 360 µm thick 2 inch diameter (100)-Fe-InP substrate. The

room-temperature epi-layer properties were measured using Van der Pauw structures giving n_{Sh} of 1.03x10^{13} cm^{-2} and μ_H of 5600 cm^2/Vs. After processing and selective wet etch removal of the InGaAs cap in a succinic acid based etch solution, room temperature values of n_{Sh} of 2.5x10^{12} cm^{-2} and μ_H of 8650 cm^2/Vs were measured.

In order to evaluate the mm-wave performance of *70 nm* HEMTs, devices were realized using the Glasgow MMIC fabrication process. *Ni-Ge-Au* based ohmic contacts were annealed at 280^{O}C using rapid thermal annealing, resulting in transistors with repeatable ohmic contact resistances around *0.15 Ω.mm*. Wet-etch mesa isolation was performed using a 1:1:100 phosphoric acid:hydrogen peroxide:water solution. The *70 nm* T-gates were realized by electron beam lithography (Leica Microsystems Lithography Ltd EBPG-5HR 100) utilizing a UVIII/PMMA resist stack [4]. Gate recess etching was performed using a selective wet chemical etch with succinic acid and Schottky gate metallisation was *Ti-Pd-Au*. Bond pad metallisation of *1200 nm Ti/Pd/Au* was used to facilitate electrical connection to the devices. A selection of two finger devices with widths in the range 40-100 *μm* were fabricated in coplanar waveguide technology, to facilitate direct on-wafer mm-wave characterization.

Figure 1 shows the measured extrinsic DC output characteristics of a *2x30 μm* 70nm T-gate device. The device has a measured peak extrinsic DC g_m of ~710 *mS/mm* at 380 *mA/mm* drain current, and a threshold voltage V_{th} of –1.4 *V*.

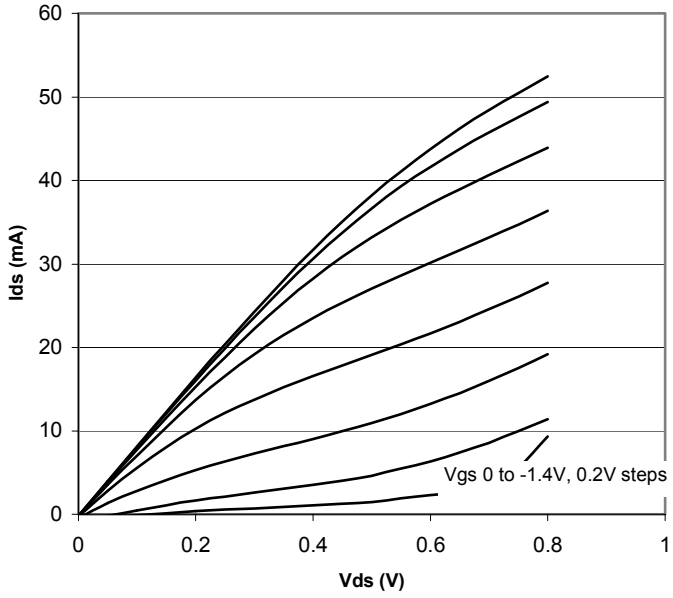

Figure 1 – Measured DC Output curves of 2x30μm 70 nm InP lmHEMT device.

On-wafer S-parameter measurements were performed from 0.04-60 GHz over the full bias range, using an Anritsu 360B Vector Network Analyser fitted with on-wafer Picoprobes from GGB. Calibration was performed using a Cascade Microtech Impedance Standard Substrate (ISS) and the LRRM technique. FET model extraction was performed at each bias point to study the performance. Figure 2 shows a plot of

measured and modelled |h21| against frequency for a *2x50 µm* gate width device biased at Vds =0.9V, Ids = 150 mA/mm. At this bias, using –20dB/decade rolloff, the device has an extrapolated peak f_T of ~300 GHz.

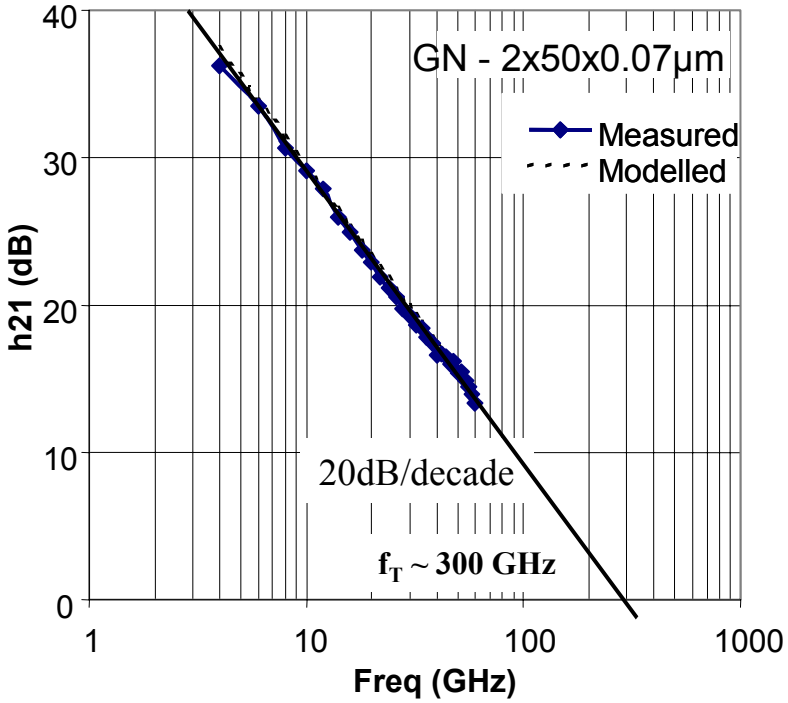

Figure 2 – Plot of measured and modelled |h21| vs frequency for the 2x50µm 70nm device at Vds = 0.9V, Ids = 150 mA/mm

CONCLUSIONS

We report the fabrication and high frequency performance of 70nm T-gate lattice matched InP HEMTs incorporating a UVIII/PMMA bilayer resist stack for gate realisation. At the 70 nm node, devices with f_T of around 300 GHz have been demonstrated. It is our belief that the UVIII/PMMA resist stack will play an important role in defining low resistance, sub-50 nm footprint T-gates in future due to the large sensitivity differences between UVIII and PMMA and the resulting process latitude this offers.

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