

A High Performance 2.4GHz Linear Power Amplifier in Enhancement-mode GaAs pHEMT Technology

Yut-Hoong Chow and Thomas Chong

Wireless Semiconductor Division, Agilent Technologies (Malaysia)

Bayan Lepas Free Industrial Zone, 11900 Bayan Lepas

Penang, Malaysia

Tel: 60-4-6430611

Fax: 60-4-6423732

Email: yut-hoong_chow@agilent.com, thomas-ck_chong@agilent.com

Abstract — This paper describes the design and realization of a high performance linear power amplifier in the 2.4GHz band for the IEEE 802.11b/g WLAN (Wireless Local Area Network) and ISM (Industrial Scientific and Medical) applications using a proprietary 0.5 μ m enhancement-mode Pseudomorphic High-Electron-Mobility Transistor (e-pHEMT) technology. The amplifier exhibits a linear power output of 18.5dBm at 5% Error Vector magnitude (EVM) and efficiency of 30% at 2.45GHz at 3.3V supply in a chip-on-board (COB) module. The design also includes an integrated power detector.

I. INTRODUCTION

With the ever-increasing demand for higher data rates in wireless applications, e.g. 802.11 WLAN, designers have an uphill challenge to design linear amplifiers to meet ever more demanding performance goals such as lower current (hence efficiency), higher power output and improved linearity. For example, the 802.11g (2.4GHz) specification enables up to 54Mbps of data rate employing Orthogonal Frequency Division Multiplexing (OFDM) 64-QAM modulation while maintaining a total system EVM of not more than 5.6%. This is a vast difference compared to current 802.11b Wi-Fi standard which provides up to only 11Mbps using Direct Sequence Spread Spectrum (DSSS) and Complementary Code Keying (CCK) modulation.

Significant improvements in this PA linearity-vs-efficiency trade-off have been realized in this respect with Agilent's proprietary 0.5 μ m GaAs e-pHEMT process [1]. This paper demonstrates that with this technology and optimum device biasing and matching, a high-linearity, high-efficiency PA (power amplifier) can be designed without resorting to fancy linearization techniques. We describe a WLAN PA that achieves 30% efficiency with a linear output power of 18.5dBm for a 54Mbps OFDM-modulated signal using a single 3.3V supply. The PA includes shutdown circuitry as well as on-chip RF power detection functionality. The chip occupies an area of 1.25mm x 0.525mm.

II. GAAS E-PHEMT CHARACTERISTICS

Typical output power vs input power curves for a pHEMT are shown in Fig. 1 below for different bias conditions. Notice both gain expansion and gain compression are possible, depending on the bias used. By a judicious combination of gain expansion and compression in a multi-stage amplifier it is possible to maximize the maximum output power while maintaining minimal bias currents in a Class A-B amplifier. This is accomplished via optimizing pHEMT bias currents and impedance matching circuitry on- and off-chip.

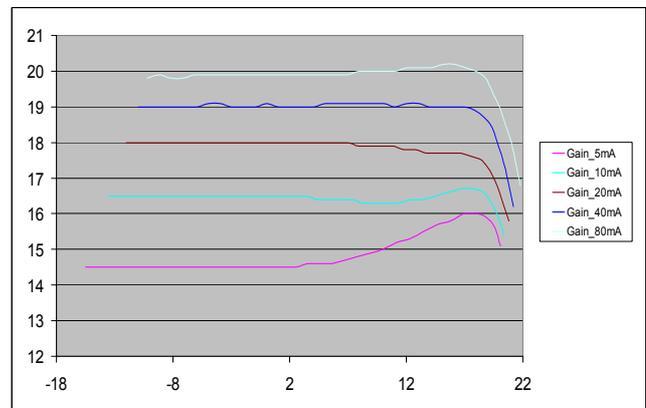


Fig. 1. Gain for different bias currents of a 800 μ m e-pHEMT

III. THE DIE-LEVEL AMPLIFIER DESIGN

Figure 2 shows the circuit of the amplifier. For brevity, the bias circuits are not shown. A single shunt inductor provides input match by resonating with the input capacitance of the 1st stage device (Q1). Inter-stage match is accomplished by means of a drain inductor at Q1, and a series inductor-capacitor between Q1 and Q2. A drain inductor and output shunt capacitor at Q2, and associated output bond wires and surface-mount capacitors form the output match. Figures 3 and 4 below show the topologies for the bias circuits and power detector respectively.

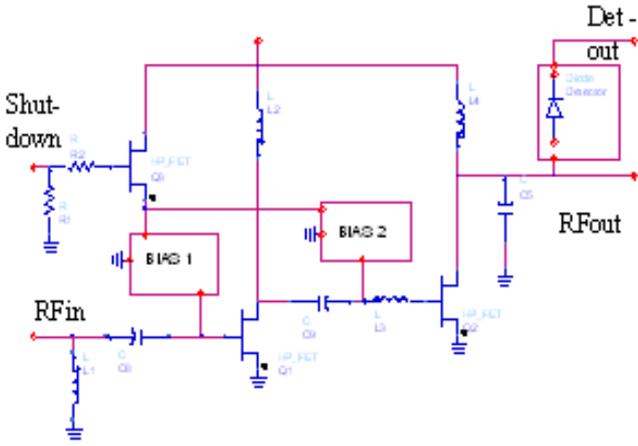


Fig. 2. Die level schematic of the amplifier

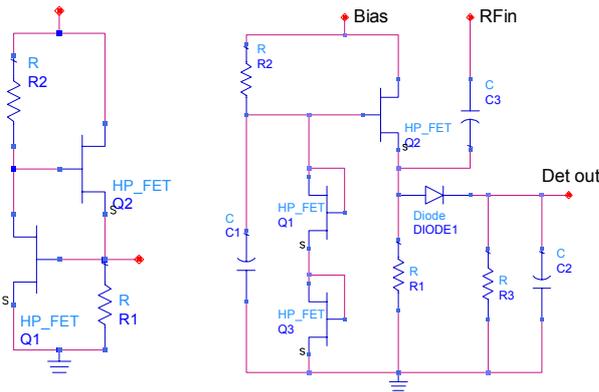


Fig. 3. Bias circuit

Fig. 4. Power Detector

each of the devices over temperature so that the voltages at the gates of the amplifying devices remain constant [2]. By selecting the bias currents and device sizes appropriately, it is possible to achieve flat gain versus output power characteristics for very high output powers close to minimal back-off of the power amplifier. In this way, the PA can operate in minimal bias class-B mode while attaining the linearity required. The actual values of the bias currents and device sizes are dependent on the process characteristics. The enhancement-mode pHEMT process used showed high linearity across a wide input power, supply voltage and bias current range. This is important to determine the maximum power output attainable for a given quiescent bias and efficiency.

The power detector is made up of a diode-connected pHEMT with current mirror bias as shown in Fig. 4. The output is almost linear with input power in dBm (see also Fig.13.)

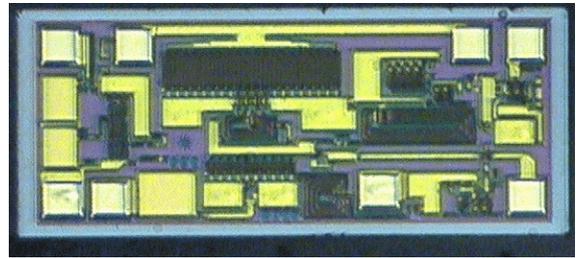


Fig. 5. Die level layout

The bias circuit consists of a dual-pHEMT self-compensating current source which tracks the changes in

Fig. 6. Simulation schematic of the amplifier with matching components, transmission lines and package parasitics.

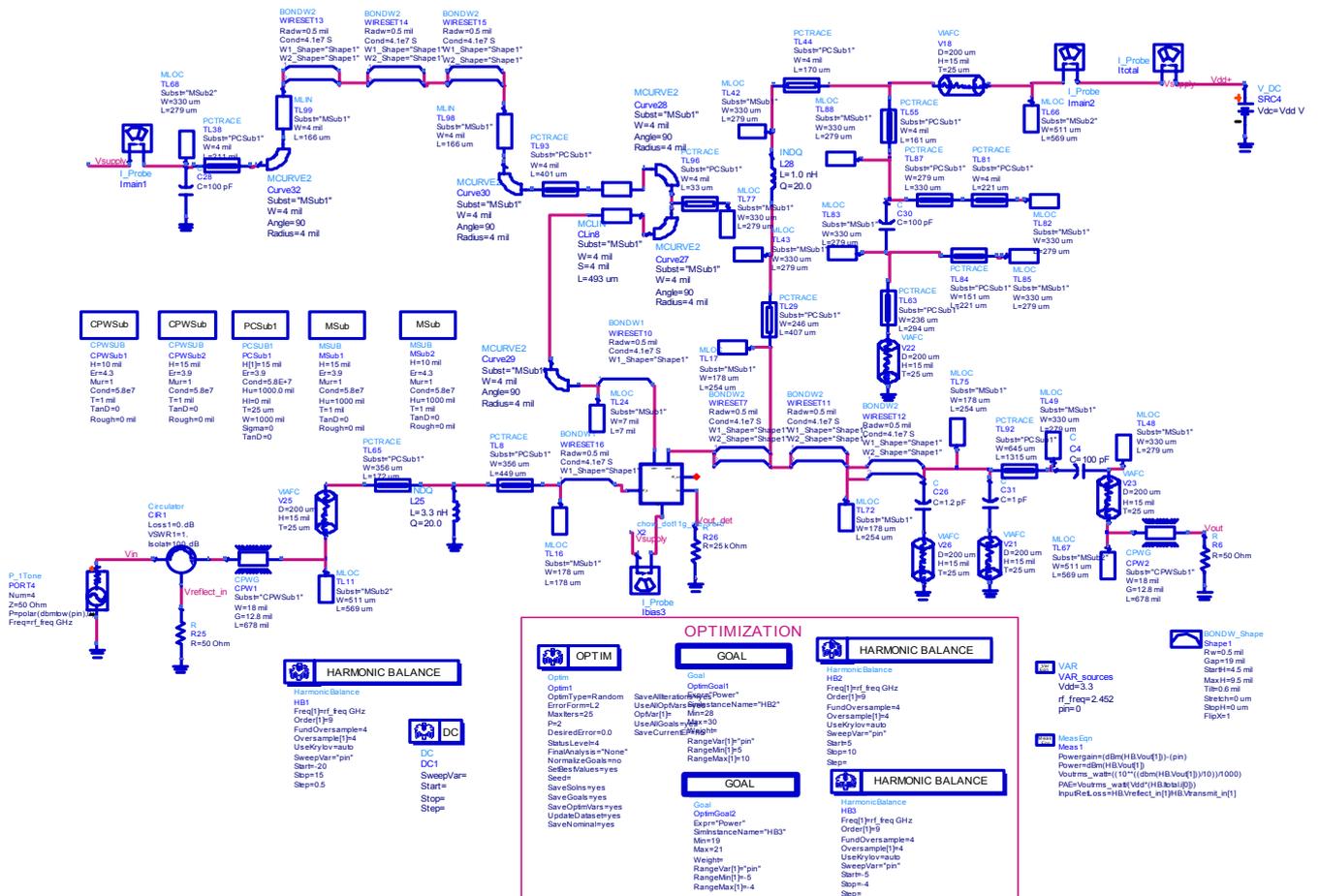


Figure 5 shows the layout of the die in Agilent's proprietary 0.5um enhancement-mode GaAs-AlGaAs pHEMT process. The die measures 1.25mm x 0.525mm.

IV. THE MODULE AND PACKAGING DESIGN

The Agilent Technologies Advanced Design System (ADS) simulator was used extensively to predict and optimize the performance when the die is packaged in a COB module. The simulation schematic was carefully constructed to include all the board traces, wirebond pads, component pads, vias and module solder pads. Agilent's Root Model [3] was used for the active devices. The simulation schematic is shown in Fig. 6 and the swept power, gain and current results are shown in Fig.7. Using the same values as that obtained from simulation, good correlation was noted for gain and power (within 1dB). For the current drain, good correlation was obtained in the trend beyond the 18dBm power output level, but not in the low level (linear) region. Nevertheless, the simulation exercise was very important in determining the matching topology and component values, thus reducing cycle time tremendously. The printed circuit board (PCB) layout is shown in Fig. 8.

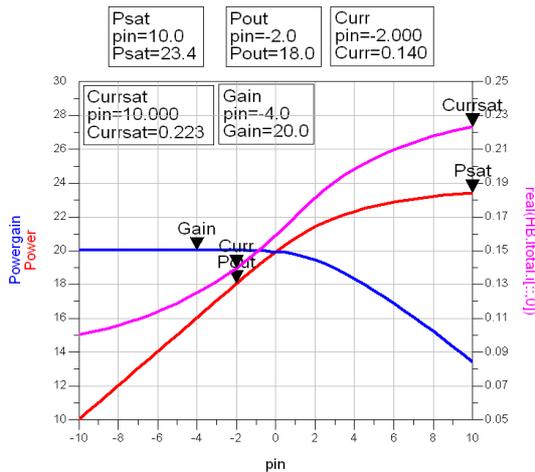


Fig. 7. Simulation results.

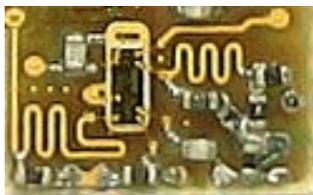


Fig. 8. PCB layout of the amplifier showing MMIC, transmission lines and matching components.



Fig. 9. Module mounted on evaluation board

The module PCB is a 0.015" thick Getek® material with a dielectric constant of 3.9. The dimensions are 5x6x1.1mm³. (Note: The module is actually bigger than it needed to be as it was designed to accommodate two circuits, but only one of the circuits is discussed here). The choice of COB over other packaging options such as plastic leadless chip carrier (PLCC) or ceramic LCC is so that the matching surface mount components can be integrated, and for cost reasons. Figure 9 shows the final encapsulated COB module mounted on a polyimide evaluation board.

V. MEASURED PERFORMANCE

The module was measured for its performance using standard techniques. For EVM measurements the OFDM signal source is an Agilent ESG 4438C Vector Signal Generator, and the analysis is performed by an Agilent E4440A Performance Spectrum Analyzer (PSA) (E444XA/AU option K70) in conjunction with Agilent 89611A Vector Signal Analyzer (VSA) 70MHz IF module. The supply voltage is 3.3V.

Results:

Frequency: 2.452GHz
 Gain: 20.6dB
 Psat/Current: 25.5dBm/203mA
 @5.0%EVM,Pout/Current/PAE: 18.5dBm/70mA/30%
 @3.0%EVM,Pout/Current/PAE: 17.4dBm/64mA/26%
 OIP3: 24dBm
 2nd /3rd /4th harmonics: 34/44/68dBc
 Input Return Loss: -19dB
 Output Return Loss: -8dB

Figures 10 and 11 show the swept-power measurements of the module. In Fig. 10, notice the flat gain, close to 21dB, up to a very high output power level (22dBm). The shape of the curves mirror that obtained through simulation (see Fig.7).

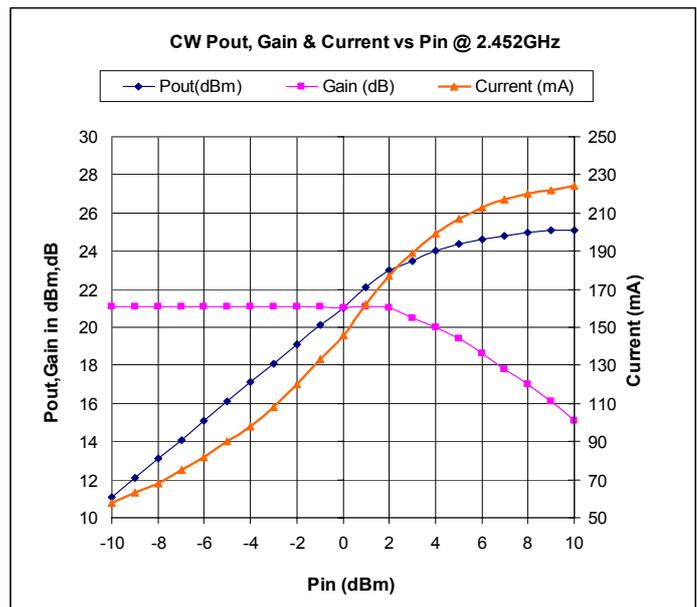


Fig. 10. Swept power measurement of the PA module

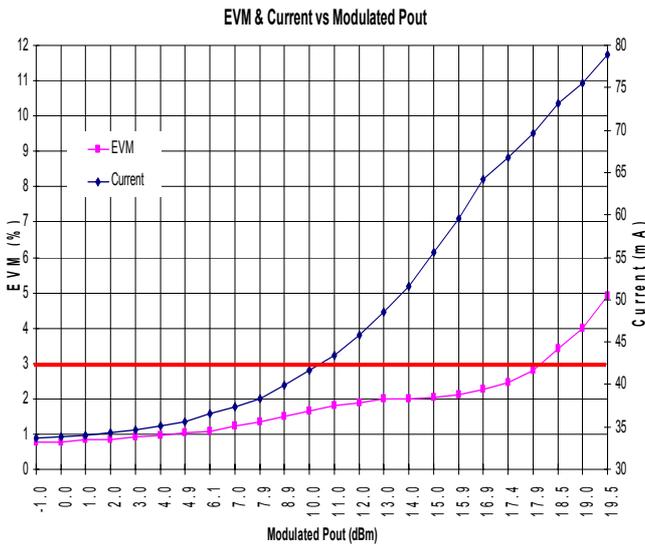


Fig. 11. EVM and current vs Pout plot of the PA module

Figure 11 show typical EVM and current vs Pout curves. Typically, at 3% EVM, the Pout is 17.0 to 18dBm. At 5% EVM, the Pout is 18.5 to 19.5dBm with a 70 to 80mA current drain. Figure 12 below shows the modulated signal measured using the WLAN analyzer. Finally, the power detector output versus power is shown in Fig. 13 which shows a high degree of linearity.

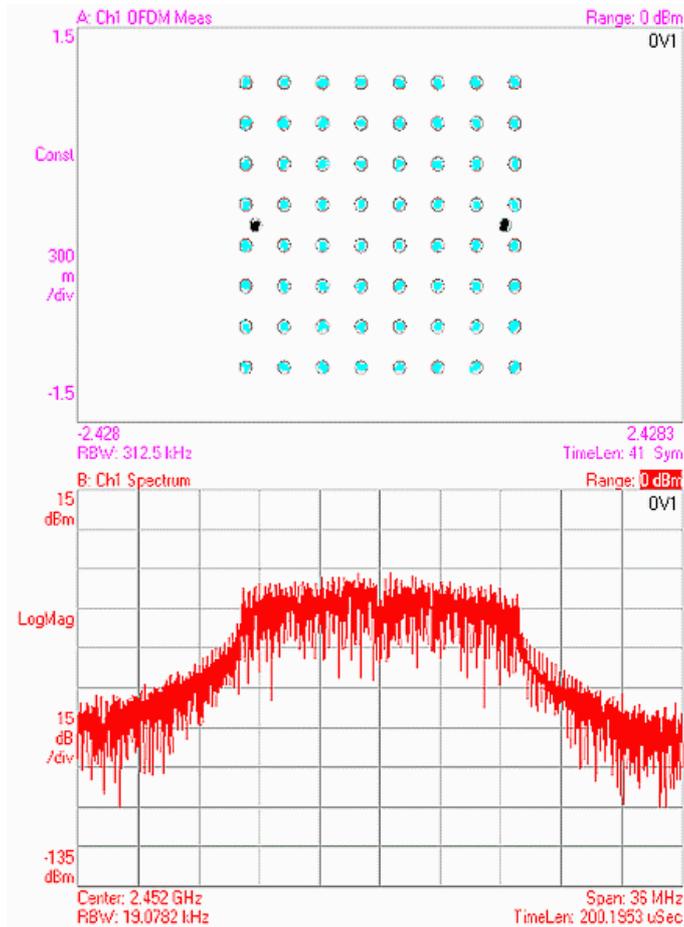


Fig. 12. Plot of PA module output at Pout=+18dBm @EVM=3% with 802.11g 54Mbps 64-QAM OFDM modulation

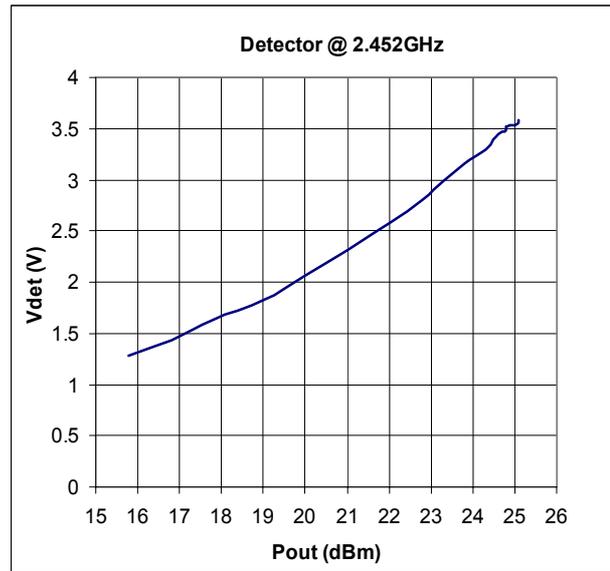


Fig. 13. Plot of detector output vs output power

VI. CONCLUSION

The design and measured performance of a high-linearity, high-efficiency power amplifier at 2.45GHz employing Agilent's proprietary GaAs e-PHEMT fabrication technology has been presented. The power amplifier was designed primarily for the IEEE 802.11g WLAN standard employing OFDM modulation at 54Mbps. With internal matching, an easy-to-use module has been realized giving 21dB gain with a 2-stage topology. An unprecedented efficiency of 30% at a linear output of 18.5dBm, at 5% EVM, has been demonstrated. This level of performance holds good potential for current-constrained products like WLAN NIC cards, and wireless-enabled Personal Digital Assistants (PDA).

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