A High Performance Yet Easy to Use Low Noise Amplifier in SMT Package for 6 to 20 GHz Low Cost Applications

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***Abstract* – This paper describes a groundbreaking 6-20 GHz Low Noise Amplifier (LNA) that is easy to use, high performance and low cost. For ease of use it incorporates a 5x5 mm surface mount package, self-biasing, operate on a single 3V supply, and integrated 50 Ω input/output matching. For performance the package amplifier delivers over 20 dB gain and 2.1 dB noise figure. Cost is kept low through utilization of PHEMT 6" wafers and volume automated package panel assembly and test. The authors feel this product is unique and industry leading in all aspects of design, packaging performance and cost.**

I. INTRODUCTION

Commercial radios operating in the 6-20 GHz bands for Point-to-Point, LMDS, and satellite communication applications require Low Noise Amplifiers (LNA) as the first amplification stage on the incoming signal. Narrow band LNAs can be built using Field Effect Transistors (FET) and hybrid, on-board matching and bias networks. However, such systems are design-intensive, hard to change, and require high piece part inventories. The usage of a single integrated LNA simplifies design and part inventory. By having one wide band LNA, the design resources and inventory can be reduced since it covers many commercial frequency bands. The system buyer can negotiate better pricing on larger volume of one part rather than many piece parts. Last, fewer parts allow easier quality monitoring and more reliable final assemblies.

This paper describes a single MMIC that provides such a solution. As a wide band LNA it can be used for either primary or sub sequential low noise gain stages. It was developed to provide a low cost product for many systems and frequency bands. It replaces cumbersome balance MIC FET LNAs and hybrid chip-and-wire MMICs with a clean surface mount solution. The high-performance package helps enhance the handling and assembly process while preserve the broadband low noise performance. Costs are kept low by employing volume GaAs PHEMT 6" wafer process and modern laminate package. The LNA is a true enabler for future low cost systems covering 6-20 GHz.

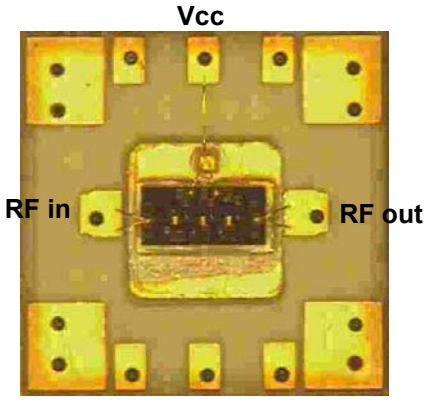

Figure 1. A 6-20 GHz PHEMT LNA MMIC in a SMT package (lid removed).

II. PROCESS DESCRIPTION

To realize this LNA a low 0.15u gate Pseudomorphic High Electron Mobility Transistor (PHEMT) was selected. This is due primarily to the excellent minimum noise figure available with realizable Γopt and Rn parameters for these bands. It is very important for the process to have a small gate and thus small parasitic gate capacitance since impedance movement across the Smith chart must be minimized in a wide band applications.

The foundry used is a modern facility capable of high volume, high yield, and 6-inch wafer production. With typical gate sizes of 0.15μm and F_T of 70 GHz this process is well capable for this application. Typical process guaranteed specifications are shown in Table 1. The process is equipped with passive components which include 50Ω/ Thin Film Resistor, 213 Ω/ bulk resistor, 0.4fF/μm^2 Si_3Ni_4 MIM capacitor, 27pH backside via, and two metal layers for transmission lines.

TABLE 1. TYPICAL PHEMT PERFORMANCE

Parameter	Unit	Min	Typ	Max
I_{DCmax}	MA/mm	400	500	600
Gm	MS/mm	425	495	570
Vgs@Peak Gm	V	-0.7	-0.45	-0.2
Vpo	V	-1.3	-1.0	-0.7
Vgd,bd	V	8	11	15
Ft @ 1.5V	GHz	70	85	100
Psat	dBm		28	
PAE	%		56	
Gain	dB		19	

III. LOW NOISE AMPLIFIER DESIGN

The LNA is comprised of 3 cascaded gain stages. Each gain stage is self-biased where the DC biasing condition is set by the resistor at the source end of the FET and the biasing resistors are bypassed by large capacitors. The self-biasing technique not only helps eliminate the need for negative supply, but also ensures a low noise performance by preventing any intrinsic noise sources of the negative voltage generator from getting to the FETs. For optimum noise performance, the DC current Idd in the first stage is chosen to be approximately 15% of the Idsat, and the following stages' Idds are chosen to give the overall necessary gain requirement. The three stages are biased from two 3V supplies with some internal bypassing capacitance and de-coupling resistors.

Figure 2 shows the micro-photograph of the low noise amplifier. A simplified schematic diagram is shown in Figure 3. It consists of 3 gain stages, low noise design with a 6-finger 265µm E-PHEMT in the first stage and 6-finger 250µm E-PHEMTs in the final 2 stages. The first stage usually determines the overall noise performance of the entire design; therefore, a tuned transmission line is used to optimize the noise and input match at the same time. Each stage has a certain drain inductance to improve the inter-stage match for better noise and gain performance at the high end of the bandwidth. A small amount of negative feedback is used at the input stage to help with broadband match. Negative feedbacks were also utilized at the final 2 stages to help flatten the gain response. To further flatten the gain response, a built-in equalizer at the gate of the final FET is employed. The equalizer consists of the gate inductance in series with a parallel combination of a 50Ω resistor and a capacitor. This equalizer is employed at the final stage, to be as far away from the first stage as possible, not to disturb the optimum match at the input. The final two stages provide broadband gain, therefore, any inductance at the FETs sources were intentionally kept to a minimum through layout technique and the utilization of backside via.

To reduce the effect of process variations on noise performance and DC current consumption, the width of the biasing resistors are made quite large. This will keep the DC currents in each stage as constant as possible from wafer to wafer.

For system application the LNA is simple to use. The MMIC has full DC blocks on input and output; integrated RF choke; and self-biasing for single 3V supply operation. Stability and proper 50-Ω match are guaranteed 2:1 for 7-20 GHz with integration. Narrowing the bandwidth the frequency range can be taken down to 6 GHz with a small addition of input inductance There is little part to part variations since the design is simple and every MMIC is printed and processed the exact same way to demanding standards.

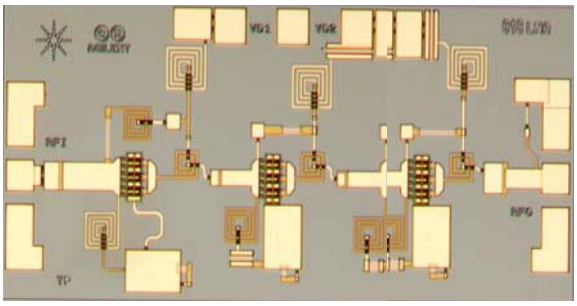

Figure 2. Layout of the LNA (1.7mm x 0.8mm)

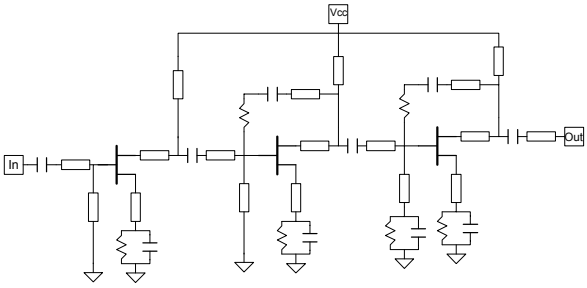

Figure 3. A simplified schematic for the LNA

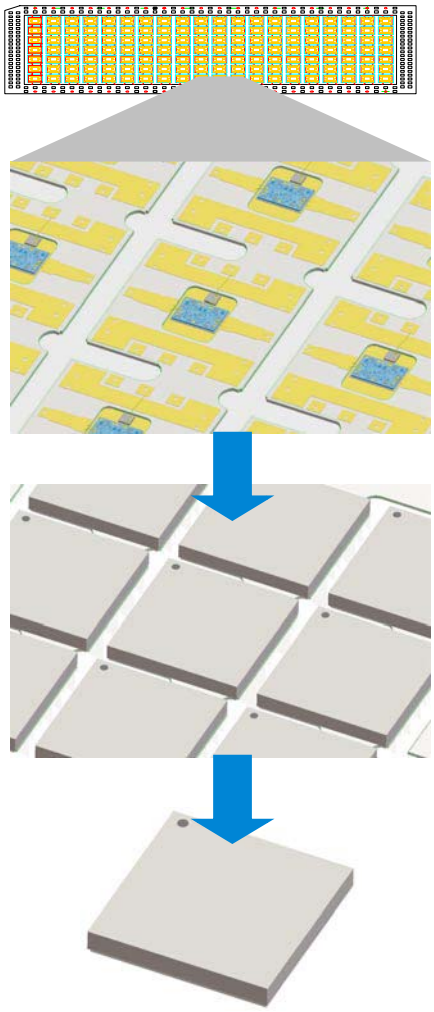

Figure 4. Assembly process into Package

IV. PACKAGE

The package is designed to be assembled and tested in panel form to keep costs low. Panels are manufactured with Rogers 4350 material with metal backing it is fully compatible with modern module assembly lines. Each package is divided into a 5x5mm dimension for die placement and bonding. The lids are then attached and each MMIC is tested for full bandwidth performance. Finally the MMICs are divided and loaded into tape and reel. The whole process is automated and capable of millions of units per month.

The I/Os of the package are designed using extensive EEsof HFSS simulations to ensure proper system board micro-strip to package micro-strip transition. The package is capable of maintaining better than 15 dB return loss to 40 GHz. Each MMIC is characterized to carefully documented reference plan set point to ensure performance accuracy in the customer application.

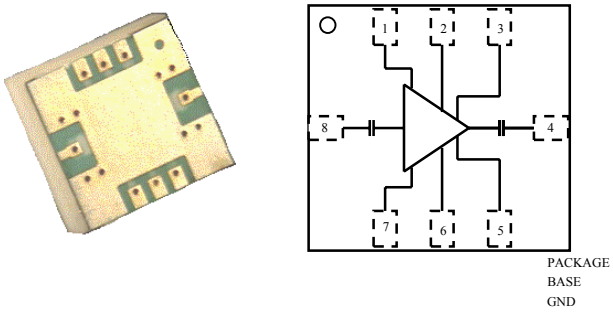

Figure 5. Final part (shown from bottom)

V. MEASURED RESULTS

The final packaged LNA is 100% tested at microwave frequencies on a automatic tester. Individual performance measurements were made using a demonstration board as shown in figure 6. The demonstration board uses a coplanar wave launch into the package and 2.4mm connectors for clean wide frequency band performance. Measurements are made on a Agilent 8510 Network Analyzer and 8970 Noise Figure Meter.

S-parameter results are shown in Figure 7 for Gain, Return Loss and Isolation. The gain is very flat and in the 21 to 23 dB range across the entire band. Output return loss is better than –10 dB (2:1 VSWR) across the entire band while input return loss rises to –8 dB (2.3:1) only from 6-7 GHz.

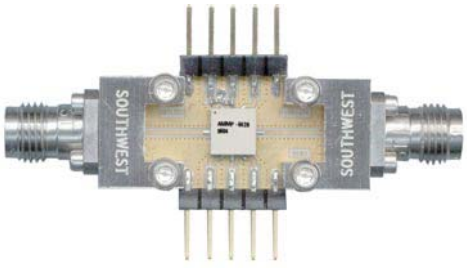

Figure 6. Demonstration test board.

be improved a small amount of external series Input return loss at low frequencies can inductance. Isolation is generally 38 dB or better or at least 15 db over gain to help insure unconditional stability.

Figure 8 shows typical noise figure over frequency. For 7 to 13 GHz the noise figure is below 2 dB and all other bands the noise figure is below 2.5 dB. The noise figure into a 50 Ω load is generally .2 to .3 dB worse than the optional noise figure (Gamma Opt). This demonstrates that the amplifier is very well designed to bring both s11 conjugate and Gamma Opt at or near the 50 Ω point.

Figure 9 shows the typical noise figure change over temperature. The noise figure generally changes in direct proportion to the GaAs PHEMT intrinsic transconductance and noise generation change rather than movement of Gamma opt. or s11.

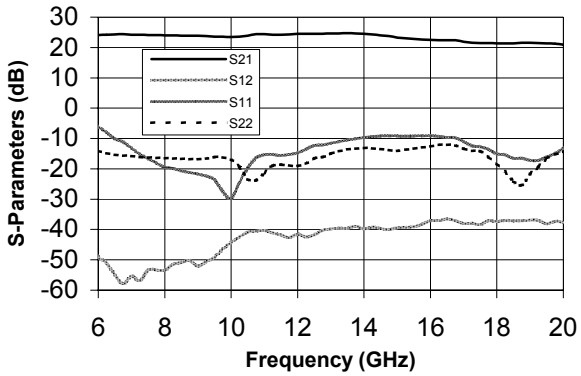

Figure 7. Typical measured Gain, RL and Isolation

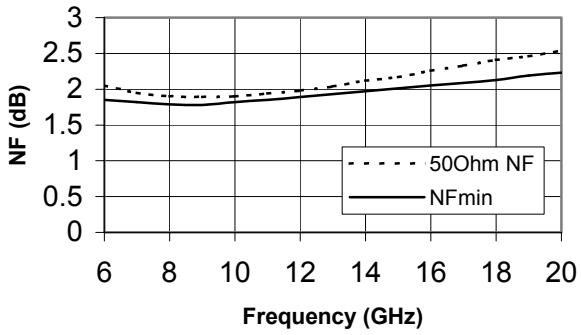

Figure 8. Typical Noise Figure (into Γ_{opt} and 50 Ω)

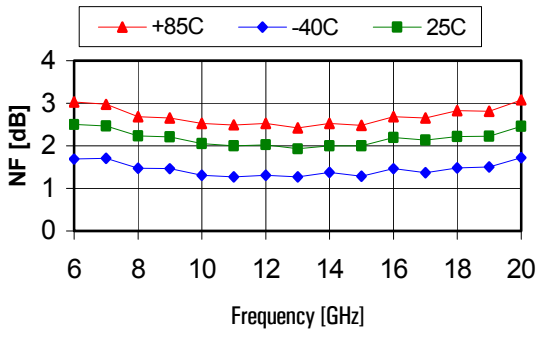

Figure 9. Typical Noise Figure over temperature

V. SUMMARY

This paper has described a 6-20 GHz Low Noise Amplifier (LNA) that is easy to use yet delivers high performance. The designed LNA provides over 20 dB gain and less than 2.5 dB noise figure 6-20 GHz. It's easy to use since it integrates the 50 Ω input and output match and has the ability to operate on a single 3V supply with no negative bias voltage required.

While simple to use the LNA utilized many advanced technologies. A 0.15µm gate PHEMT process with 70 GHz Ft is used for low noise amplification. The three-stage design used integrated self-bias and loaded source inductance combined with feedback to lock Γopt at or near 50 Ω impedance wide band to ensure low noise. The package uses state-of-the-art material and innovative three-dimensional modeling to minimize signal loss.

Last, the product is made with volume and low cost as a prime design criterion. The MMIC is processed on large 6" wafers with high-speed e-beam and stepper lithography. The package is panel processed through assembly and test to allow total automation.

This MMIC has the unique combination of bandwidth, performance, package and low cost. Research products such as this are true enablers of lowering the barrier to volume applications above 6 GHz.

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United Kingdom: Alan Rixon, Robert Brophy

TABLE 2: SUMMARY OF PERFORMANCE

Symbol	Parameter	Unit	Typ	Min/ Max
V_D	Drain Supply Voltage	V	3	
I_D	Drain Supply Current	mA	52	
Gain	Small-signal Gain	dB	22	19
RL_{in}	Input Return Loss	dB	-13	-9
RL_{out}	Output Return Loss	dB	-15	-10
Isolation	Reverse Isolation	dB	-45	
NF	Noise Figure	dB	2.1	2.5
OIP3	Output 3rd Order Intercept Point	dBm	+20	

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