Design Procedure and Performance of two 0.5-20 GHz GaAs PHEMT MMIC Matrix Distributed Amplifier for EW Applications

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***Abstract* — Two monolithic matrix amplifiers for ECM and ESM military equipment have been designed and realized using 0.25 μm GaAs PHEMT technology from UMS. Design trade-offs and performances are discussed in detail. The effects of the biasing network, termination load and total gate periphery on the performance of the amplifiers were considered for optimum design. The first amplifier , designed for gain flatness and noise figure yields gain of 19 ± 1 dB and a typical noise figure of 4 dB. The second unit exhibits a positive linear gain slope from 16 dB to 20 dB. Output power at 1 dB compression point is +12 dBm. The die size and bandwidth of each MMIC is 7 mm^2 and 0.5-20 GHz respectively.**

I. INTRODUCTION

Broadband amplifiers are required in applications such as modern Active Phased Array Radar Systems, Electronic Warfare Front Ends and High speed Optical Transmission Systems. The use of the Matrix distributed amplifier, proposed by Niclas [1], is a very good choice thanks to an effective combination of high gain (additive and multiplicative amplification principle in one and the same module), wide bandwidth and reasonable noise figure in a compact die size. A methodology for the design of low noise, power and driver matrix amplifiers has been outlined, with the aim to obtain a trade-off solution for the specific application.
To validate the design method used, we have designed, fabricated and measured two 2x4 MMIC Amplifiers based on MMIC PH25 P-HEMT UMS foundry process.

II. CIRCUIT DESIGN

In its general form, the matrix amplifier is formed by m rows and n columns of active devices. In case of two tiers of active devices, the matrix amplifier can be decomposed into three artificial transmission lines, namely the *input*, the *central* and the *output* ones. Otherwise, from a different point of view, the matrix amplifier can be decomposed into three identical Tschebyscheff filters that can be designed using ladder network filter theory [2]. In this paper transmission line theory will be used.

To satisfy the distributed amplification principle, the three artificial transmission lines shall have the same phase velocity and the same cutoff frequency. Moreover, input and output matching conditions may be obtained according to the following expressions:

$$Z_{0in} = \sqrt{\frac{L_g}{C_{gs1}}} = Z_{0out} = \sqrt{\frac{L_d}{C_{ds2} + C_{add}}} = 50\Omega = Z_0 \quad (1)$$

$$v_{Pin} = \frac{1}{\sqrt{L_g C_{gs1}}} = v_{Pout} = \frac{1}{\sqrt{L_d (C_{ds2} + C_{add})}} \quad (2)$$

$$v_{Pc} = \frac{1}{\sqrt{L_c (C_{gs2} + C_{ds1})}} = v_{Pin} = v_{Pout} \quad (3)$$

From (1) and (2) we obtain:

$$L_g = L_d = L = 50^2 C_{gs1} \quad (4)$$

$$C_{gs1} = C_{ds2} + C_{add} \Rightarrow C_{add} = C_{gs1} - C_{ds2} \quad (5)$$

Where from (3):

$$L_c = \frac{1}{\pi^2 f_c^2 (C_{gs2} + C_{ds1})} \quad (6)$$

$$Z_{0c} = \sqrt{\frac{L_c}{C_{gs2} + C_{ds1}}} \quad (7)$$

Where C_{gs} and C_{ds} are FET equivalent circuit elements (Fig. 1); C_{add} indicates an extra shunt capacitor, added on output drain line terminals since C_{gs} is always greater than C_{ds}; L_g, L_c and L_d are the connecting inductors on input, central and output line respectively. The first step in the design process resides in the selection of an appropriate transistor technology, such as HEMT or BJT. In order to obtain a large Gain-Bandwidth product, a GaAs PHEMT device seems to offer the best compromise. In fact, thanks to its small input resistance (R_{gs}) and capacitance (C_{gs}) it exhibits a large G_{meff}/C_{gs}

ratio, as compared to a bipolar technology. The last one, however, exhibits a large G_m and a low power consumption.

A study concerning the attenuation along the three artificial transmission lines, proposed in [3], reveals that the values of R_{gs} and C_{gs} shall be as small as possible, since they impact the amplifier bandwidth; on the other hand, the values of R_{ds} and C_{ds} impact the low frequency gain: they shall be as large as possible.

The Design-oriented FET unilateral model and a graphical design procedure reported in [4] has been used to take into account high frequency parasitic effects and to quickly predict the amplifier's 3-dB cutoff frequency and the low frequency gain. Fig.1 shows the lossy device linear model used during the design.

PHEMT equivalent circuit element values (including noise parameters) can be varied, by the designer, changing bias point and total gate periphery. The optimisation of the above elements impacts directly on required performances such as gain, matching, noise figure and output power level.

Amplifier's noise performance is in fact mainly influenced by the first tier of active devices and gate termination impedance, that become a very important design tool [5] .

Depending on the application, the effects of different bias or load networks on the performance of the matrix amplifier was initially considered for its proper design.

As Modulator Driver: a resistive bias network can be used to guarantee baseband (DC coupled) operation. This topology causes a loss in the amplifier efficiency because of the current flowing through resistors.

As Low Noise device: a gate termination composed by a resistor shunted by an inductor or an active gate termination can be used to optimise the noise figure of the amplifier.

In Medium Power application: thanks to the custom size of each FET, the gate periphery can be optimised according to the power distribution along the two lines of the matrix amplifier; moreover a gate series capacitor to enhance the power handling can be used.

III. Simulation, Fabrication and Measurements

To show the effectiveness of the design method, the design and measured performances of two low noise matrix amplifiers using PHEMT devices for Electronic Counter Measures (ECM) and Electronic Support Measures (ESM) applications are presented.

Circuit schematic of the 2x4 Matrix amplifiers is shown in Fig.2. In both designs the FET gate widths have been optimized both for the first and second tier. The first tier periphery determine low noise performance, while the second one impacts gain and power performances. The second tier of active devices has been shifted towards the output, as reported in [6], by one position, thus increasing overall amplifier gain and decreasing the corresponding ripple.

50-ohm input and output matching networks and DC blocking capacitors have been used, to allow an easy integration into multi-chip modules. The low frequency behavior is controlled using choking inductors and blocking capacitors inside the MMIC; no external components are required to get 0.5 GHz operation

Linear and non linear simulations were performed using PH25 PHEMT UMS scalable model.

The layout of the first amplifier is depicted in Fig.3: it is a MMIC LNA with a small signal gain of 19dB±1dB, 10 dB return loss and 4 dB typical noise figure over 0.5-20 GHz. It exhibits a gain *vs*. temperature variation of 0.03 dB/°C only. A very good agreement between simulations and measurements is demonstrated in Fig. 4 and Fig. 5, where the gain and return loss performances are plotted as a function of frequency. The amplifier delivers an output power over +12dBm @ 1 dB gain compression at room temperature, as depicted in Fig. 6, and only ±1 dB variation from –40 °C to + 90 °C, while requiring 90 mA only from a +3V DC power supply (270 mW). The saturated output power is 15 dBm @ 25 °C. The die area is 7 mm^2.

The second amplifier, in Fig. 7, is a 0.5-20 GHz MMIC with a positive linear gain slope of 4 dB across the band from 16 dB to 20 dB @ 25 °C. Measured and simulated results are presented in Fig 8. The amplifier guarantees a typical noise figure of 5 dB, with a minimum of 3 dB at midband (Fig. 9). Output power at 1 dB compression point is +12 dBm (Fig.10). Saturated output power is +16 dBm. DC power consumption is 0.5 W (160 mA from a +3V DC supply).

The stability of both amplifiers has been verified during simulation using stability factor and S-probe method, and during the test over the operating temperature range –40 ÷ +90°C.

IV. Conclusion

A step by step design method has been proposed and verified by designing two low noise matrix amplifier using MMIC PH25 process based on a 0.25 um P-HEMT technology.

Experimental results, compared to simulations, show the effectiveness of the adopted design method, reaching a good compromise between gain, bandwidth, noise figure, power consumption and die size (cost) thus allowing the use of the realized chip in broadband military equipment.

References

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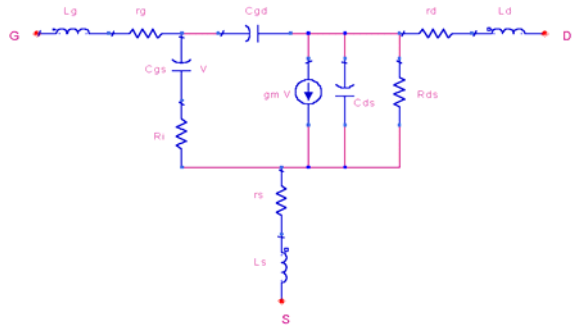

Fig. 1. Lossy active device linear model.

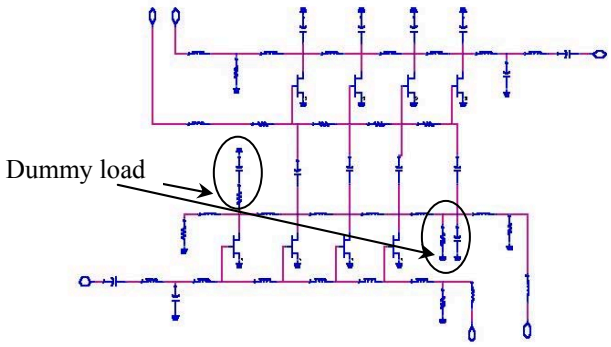

Fig. 2. Scheme of the complete 2x4 Matrix Amplifier

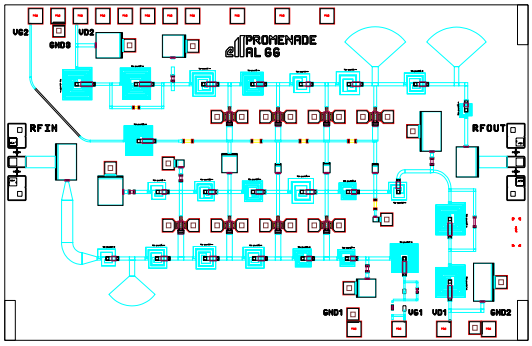

Fig. 3. Layout of the first module (Promenade).

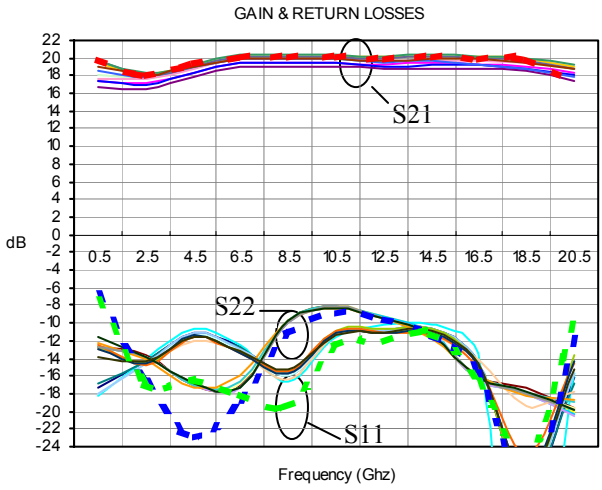

Fig. 4. Promenade on-wafer measured (continuous lines) *vs.* simulated (dotted lines) gain and return loss performances at room temperature.

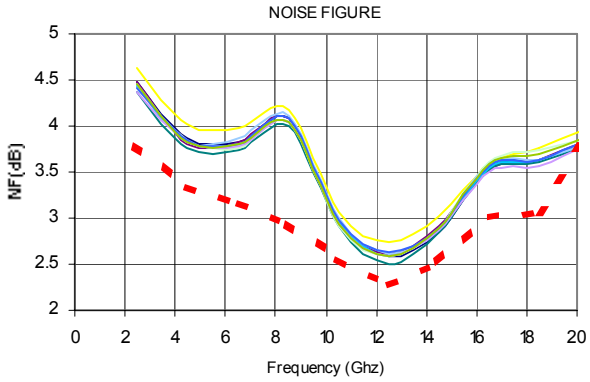

Fig. 5. Promenade on-wafer measured (continuous lines) Noise Figure *vs.* simulated (dotted lines) performances at room temperature.

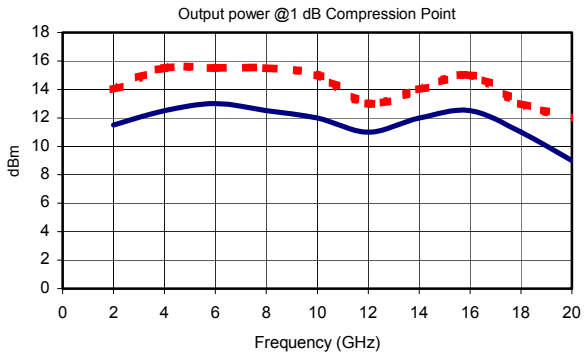

Fig. 6. Promenade measured (continuous line) *vs.* simulated (dotted line) output power at -1 dB gain compression at room temperature.

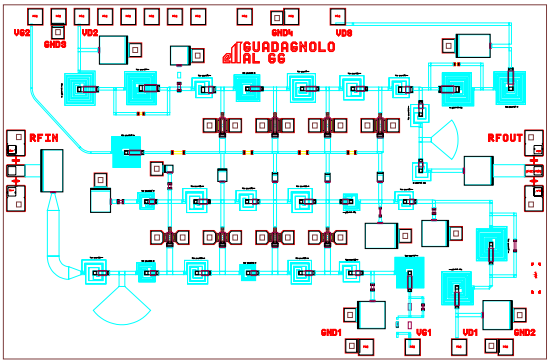

Fig. 7. Layout of the second module (Guadagnolo).

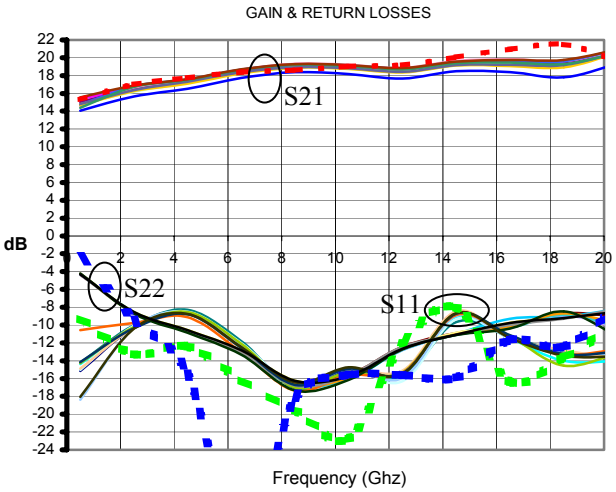

Fig. 8. Guadagnolo on-wafer measured (continuous lines) *vs.* simulated (dotted lines) gain and return loss performances at room temperature.

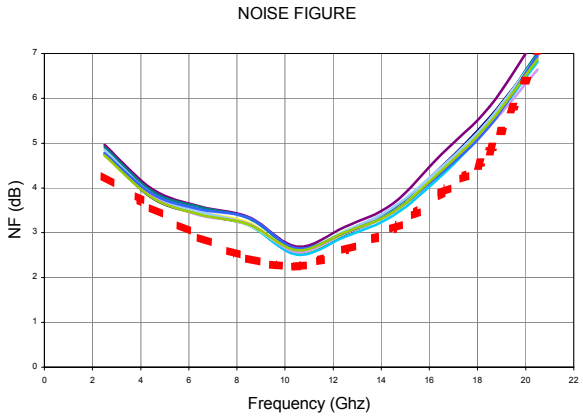

Fig. 9. Guadagnolo on-wafer measured (continuous lines) Noise Figure *vs.* simulated performances (dotted lines) at room temperature.

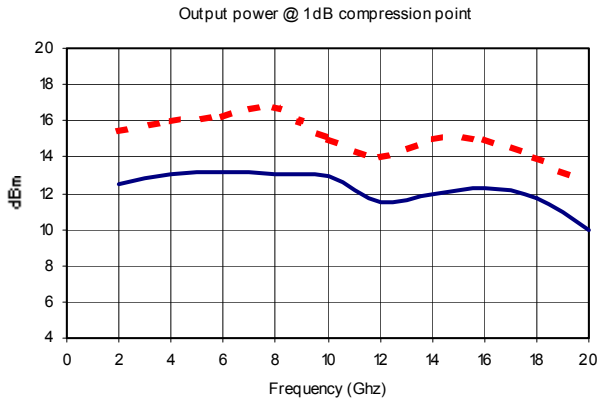

Fig. 10. Guadagnolo measured (continuous line) *vs.* simulated (dotted line) output power at 1 dB gain compression at room temperature.