Accurate Characterization of S-Band HBT Power Amplifier using simultaneously S parameters and Load-Pull Measurements

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***Abstract* — This paper emphasizes for the first time the link existing between some small-signal power gain circles and the output load of maximum power in GaAs HBTs. We use the locus of power gain, named Minimum Conjugate-Termination Power, which have the value MSG/2K. MSG is maximum stable gain and K the stability factor. This method has been applied to the measurements by load-pull of 30W S-Band HBT power bar. By varying the bias of the amplifier, it is possible using only S-parameters data to localize accurately and quickly the locus of the power load.**

INTRODUCTION

The design of high power amplifiers requires at least the optimum input and output loads. We suggest in this paper a method based on the pre- determination of the optimum safe operating area from the calculation of MSG/2K circles from S-parameters. We assess that the optimum loads for a maximum power efficiency are located inside these circles. So, S-parameters measurements show readily the area to explore in automatic load-pull, limiting the risk of destruction arising from breakdown phenomena.

II. THEORETICAL ANALYSIS

A. The Transistor as an Ideal Power Amplifier

This theoretical analysis has for purpose to determine the optimum load of an ideal amplifier. For this, a high efficiency power transistor is seen as an ideal driven source without any parasitic element as in figure 1 [2-3]. [2] has shown the optimum waveforms we must to synthesise to achieve a high collector efficiency with the control of a finite number of harmonics. With a non linear compact model of the device, we can obtain the intrinsic waveforms at the terminals of the current source as shown in figure 2. The low impedance value of the device presented during its on state forces the voltage harmonics to be set appropriately to have a collector voltage near zero volt during this period of time. This zero volt condition is best done at the driven current source terminals.

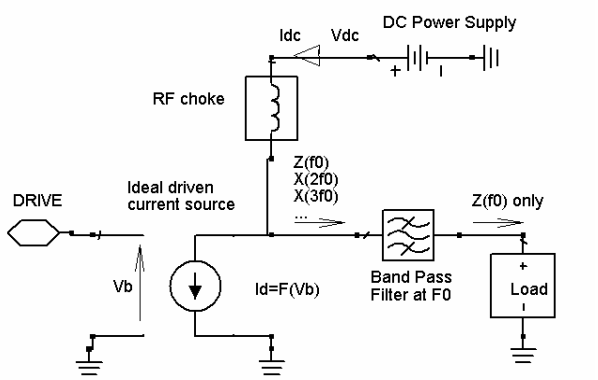

Fig. 1 Generic Power Amplifier

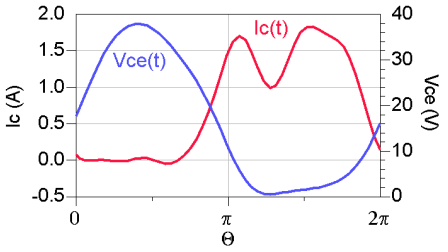

Fig. 2 Waveforms of the collector current source (Id of figure.1 or Icc of figure.3) and voltage Vce versus time at the terminal of the current source

In this example, the load at the second harmonic is an open circuit which constraints the transistors to work in class FI. Class EI is also possible. [2] describes the passage between these two classes. They give the relationship between the optimal current I_{OPT} and the voltage V_{OPT} at the fundamental and harmonics versus the DC current I_{DC} and voltage V_{DC} at the ideal current source. In all cases, the load presented at the ideal current source at the fundamental frequency is linked to the DC conductance G_{DC} defined by the ratio I_{DC} upon V_{DC}. For class FI, the conductance of the load charging the ideal current source is 1.15 divided by 1.41, $0.815G_{DC}$ and its susceptance $0G_{DC}$ for optimum result when only harmonics 2 and 3 are present [2].

B. The Transistor as an Amplifier

From a set of small signal S parameters measurements, circles of equal power gain can be drawn in the load plane. The power gain is the maximum gain achieved for a load when the input has been perfectly matched. Formulas of the power gain G_p and the stability factor K are remembered below as a function of the parameters γ, which can be z, y, h, or g network parameters,

$$K = \frac{1}{C} = \frac{2Re(\gamma_{11})Re(\gamma_{22}) - Re(\gamma_{21}\gamma_{12})}{|\gamma_{21}\gamma_{12}|} \quad (1)$$

and the load M_L:

$$G_P = \frac{M_{L,R}|\gamma_{21}|^2}{|\gamma_{22} + M_L|^2 Re\left(\gamma_{11} - \gamma_{21}\gamma_{12} / (\gamma_{22} + M_L)\right)} \quad (2)$$

From both (1) and (2), we can see that the loads y_{22}* and h_{22}* (where * is the complex conjugate) belong to the power gain circle of value MSG/2K. MSG is the maximum stable gain defined as:

$$MSG = \left|\gamma_{21} / \gamma_{12}\right| \quad (3)$$

MSG/2K as MSG and K, is invariant with any lossless passive matching circuit at the input nor at the output. It comes that the MSG/2K power gain circle is also the complex conjugate of the circle described by the output of the transistor when its input is loaded by any reactive termination including short (y_{22}) and open (h_{22}). In [4] the property that the MSG/2K is the minimum conjugate-termination transducer gain is assessed. It is equivalent because reactive termination is the minimum passive impedance possible.

As approximation, we suppose that the input and output circuits we design to match transistor for maximum performances are lossless. In this case the minimum conjugate-termination transducer gain is invariant when we match the input, so the drawing obtained with several MSG/2K circles in the load plane is invariant.

For HBT, analytical expressions of y22 and h22 can be extracted from an equivalent circuit of figure 3. We find with this equivalent circuit the following formula.

$$\mathrm{Im}ag(h_{22}) = \omega\left[C_{PC} + \left(C_{BC,INT} + C_{BC,EXT}\right)\right] \quad (4)$$

$$\mathrm{Im}ag(y_{22}) = \omega\left[C_{PC} + \left(C_{BC,INT} + C_{BC,EXT}\right)\right] \quad (5)$$

$$Real(h_{22}) = \left(C_{BC,INT} + C_{BC,EXT}\right)\frac{G_{M0}}{C_{BE}} \quad (6)$$

$$Real(y_{22}) = \omega^2 R_{BB} C_{BC,INT} \frac{G_{M0}}{1 + G_{M0}R_{EE}} Tau \quad (7)$$

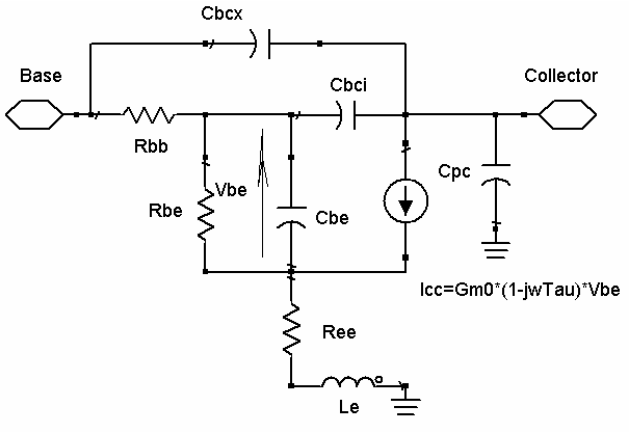

Fig. 3 Equivalent circuit used for computing y22 and h22

As already said, the MSG/2K power gain circle is the conjugate circle of the output circle when the transistor is reactively charged at the input by jBs. This last circle is described by (8). In our case this equation can be written as (9).

$$y_O = y_{22} - \frac{y_{21}y_{12}}{y_{11} + jB_S} \quad (8)$$

$$y_O = y_{22} + \frac{j\omega C_{BC}G_{M0}(1 - j\omega\tau)}{Re(y_{11})(1 + G_{M0}R_E) + j\omega C_{BE} + jB_S(1 + G_{M0}R_E)} \quad (9)$$

When Bs varies positively, one goes from h_{22} to y_{22}. The imaginary part of y_o varies little around $(C_{PC}+C_{BCINT}+C_{BCEXT})\omega$. The admittance varies from $Re(y_{22})$ to $Re(h_{22})$. This part of circle describes the low capacitance side of the circle. When Bs varies negatively, the second term goes through a maximum and y_o becomes large also.

By decreasing the base collector voltage, the power gain circle is pushed to the low base collector capacitance. At the opposite, the conductances of h_{22} and y_{22} are largely different. At low collector current, the transconductance is low as well the cut-off frequency of current gain. Power circles of low collector current shows the low conductance side. So with four circles we are able to know the side of low base collector capacitances and the side of low output conductances.

For HBTs power transistors, it exists a relationship between breakdown voltage, maximum current, and cut-off current gain frequency. We use the analysis given in [5] for the conception of power HBTs transistors to found G_{DC}. The collector layer thickness W_c is linked to doping collector level N_D. for optimal breakdown. BV_{CE0},the common emitter breakdown, is commonly around one half the common base breakdown voltage BV_{CB0}due to DC current gain value choose. I_{MAX} is the maximum collector current limited by Kirk effect. [5] obtains equation 10 to 13 for designing class A HBTs.

$$W_C \cong \frac{\varepsilon E_m}{2qN_D} \quad (10)$$

ε and E_m are the dielectric permittivity and the maximum electric field of the collector. V_{SAT} is the electron saturation velocity in the collector. A_E is the emitter area.

$$G_{DC} = \frac{I_{DC}}{V_{DC}} = \frac{\frac{1}{2} I_{MAX}}{\frac{1}{2} BV_{CE0}} = \frac{\frac{1}{2} I_{MAX}}{\frac{1}{4} BV_{CB0}} \quad (11)$$

$$I_{MAX} = qN_D A_E v_{SAT} \quad (12)$$

$$BV_{CB0} = \frac{1}{2} E_m W_C \quad (13)$$

A_C is the collector area. As the collector transit time is the main contribution to the electron transit time at high current, the cut-off current gain pulsation ω_T at high current and high voltage and the minimum base collector capacitance when collector is depleted by high voltage are introduced.

$$C_{BC,MIN} = \frac{\varepsilon A_C}{W_C} \quad (14)$$

$$\omega_T = \frac{2\pi v_{SAT}}{W_C} \quad (15)$$

$$\frac{I_{DC}}{V_{DC}} = \frac{8}{2\pi} \frac{A_E}{A_C} C_{BC,MIN} \omega_T \approx 0.424 \times Real\left(h_{22}\ \min\right) \quad (16)$$

The ratio of surface is near to 0.33. The h_{22}min is obtained at high output current when collector transit time dominates emitter transit time and high output voltage when collector layer is fully depleted.

III. Experimental verification

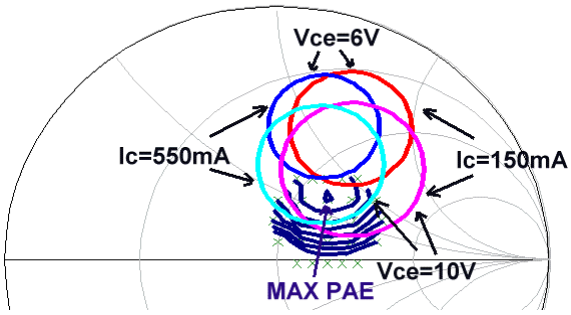

Fig. 4. Output Smith Chart with the four power gain circles issued from four small signal S parameters and Load Pull Figure at 3.1GHz

The figure 4 shows the four MSG/2K power gain circles and the power load pull contours.

Power measurements have been made on a 30W S-Band HBT power amplifier in pulsed mode at 18Volts@3.0A, at a frequency of 3.1GHz.

The four power gains MSG/2K obtained at low collector current, middle collector current, low collector voltage, middle collector voltage, are shown. The load-pull points described by automatic power bench are shown. The point of maximum power added efficiency obtained at high power is shown. Its relative position versus MSG/2K circles doesn't change in first approximation with frequency and modification of matching circuit at it can be seen in figure 5.

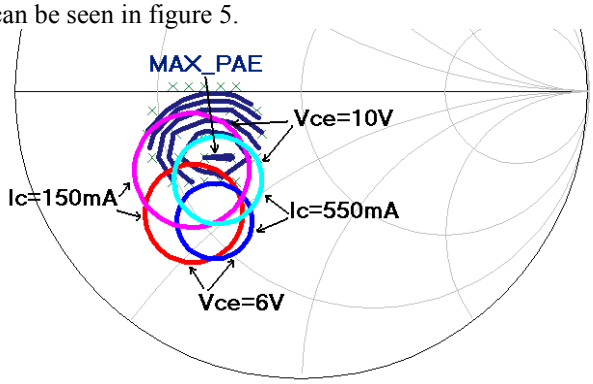

Fig. 5. Output Smith Chart with the four power gain circles issued from four small signal S parameters and Load Pull Figure at 3.3GHz.

IV. Conclusion

We presented an experimental method which links the S-parameters measurements and load pull measurements. This link allows to separate variations due to the circuits of adaptation from variations due to transistors. The change of the position of all the contours together can be attribute to the circuits of adaptation. As the S parameters measurements which can be made in CW are easier and more accurate, it can be ascertain more easily that the variations of the performances have to be attributed to passive parts or active parts of the amplifier.

Acknowledgement

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