DC and Low Frequency Noise Characteristics of SiGe n-MODFET's.

A.Rennane[1,2], L.Bary[1], J.Graffeuil[1,2], R.Plana[1,2].

[1] LAAS-CNRS, 7 avenue du Colonel Roche - 31077 Toulouse.
[2] Université Paul Sabatier, 118 route de Narbonne - 31078 Toulouse.
arennane@laas.fr, Phone : 00-33-5-61-33-62-09

***Abstract* — This paper presents an investigation of the low frequency noise properties of SiGe based n MODFET's through the characterization of both the gate current noise and the drain current noise including their correlation. Measurements versus bias and gate geometry have shown that this noise is generated through mobility fluctuations or carrier diffusion at the gate terminal and that carrier number fluctuations are involved in drain current fluctuations. Microwave residual phase noise measurements have shown that the up-conversion effect mainly occurs on the drain current noise.**

I. Introduction

The Si/SiGe heterojonction bipolar technology has been extensively demonstrated with devices featuring cut off frequencies in excess of 200 GHz and through monolithic integrated circuits both in the microwave and millimeter wave range [1,2]. The emergence of Si/SiGe Modulation Doped Field Effect Transistors (MODFET's) is more recent due to a higher complexity of the technological process (i.e relaxed buffer). Nevertheless n-MODFET's and p-MODFET's with very attractive electrical and noise performances have already been demonstrated [3-6]. It has also been reported that these devices exhibit improved low temperature performance which make them candidate for specific low noise application. However there is still a lack of an exhaustive investigation of the low frequency noise in these devices in order to know if they could be good contender for low noise non linear applications (i.e low phase noise oscillator or amplifier or low IF mixer).
In this paper, we report and comment the low frequency noise (LFN) exhibited by these devices. In next section II we present a brief description of the technology used for processing the devices under discussion and we show some of their I(V) properties. Section III concentrates on the low frequency noise characterization performed on devices featuring different dimensions with different bias conditions. Finally, section IV outlines the conclusions of this paper.

II. Technology, Description and Static Behavior

The investigated devices were n-type MODFET's designed and fabricated at the Daimler Chrysler Research Center. The core of structure is a 9 nm thick undoped pseudomorphic Si channel which is tensile stressed. It is embedded between two unstrained Sb doped $Si_{0.6}Ge_{0.4}$ spacers. The layers are grown through a LEPECVD process (Low Energy Plasma Enhanced CVD). Figure 1 illustrates the device layer structure. The technology uses a Silicon p^- substrate with $\rho > 1000$ Ωcm. More details about the device technology are given in [6].

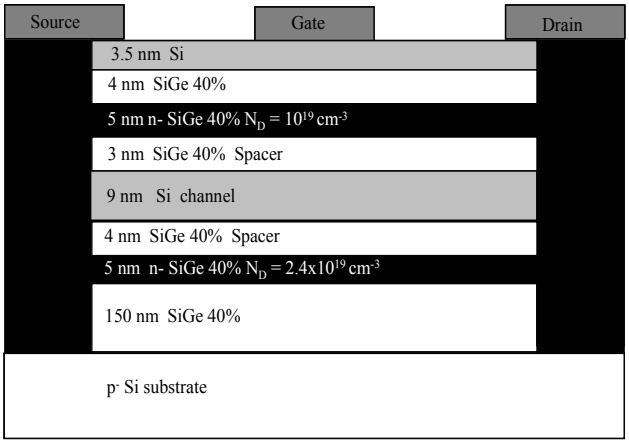

Fig. 1. Layer structure of n-type MODFET on 40%LEPEVCD.

On-wafer I(V) and LFN measurements have been carried out on devices featuring different gate length (0.1, 0.15, 0.25, and 0.5 µm) and different gate width (30, 50 and 100 µm). I(V) measurements have been carried out in order to obtain a general electrical signature of the devices, to extract their key parameters and to check the possible presence of parasitic effects (Kirk effect). Figure 2 shows the I-V characteristics of 2x50 µm gate width, 0.15 µm gate length n- type MODFET at 300°K.

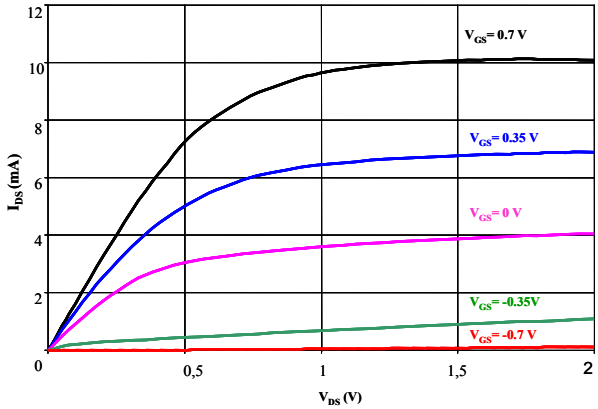

Fig. 2. I-V Characteristic of Si/SiGe 0.15µm n-type MODFET.

The devices under investigation are able to provide a drain current of 100 mA/mm at V_{GS} = 0.7 V. The transconductance scales well with the gate width and its maximum value is gm_{max} =165 mS/mm at V_{DS}= 0.5V.

We will refer to these I(V) measurements to discuss the low frequency noise behavior that will be presented in the next section.

III. SiGe MODFET'S LOW FREQUENCY NOISE

A. Low Frequency Noise characterization technique

A transistor is a two port device and an exhaustive noise characterization necessitates the measurement of two noise generators including their correlation. Different methods are available. One consists in output noise measurements for various input terminations and in referring the noise to the input through an appropriate numerical method that provides an equivalent input noise voltage generator V, an input noise current generator I and their correlation. This technique called "multiple-impedance" technique is very popular for high frequency noise figure characterization. It is also effective for LFN noise investigations in bipolar devices. Nevertheless, for LFN noise in FET devices, this method is not very easy to implement as it is understood that the LF gate current noise of a FET device is very low and the technique would necessitate inapplicable too high input terminations. It is also understood that gate current noise investigation is a very interesting tool to assess the quality of the Schottky contact. For these reasons, we have developed a dedicated test set that is able to measure the gate current noise, drain current noise and the correlation.

The set-up measures directly the AC short-circuited gate noise current i_G, drain noise current i_D at the transistor input and output terminals using two transimpedance current amplifiers. This set-up additionally allows coherence γ measurements between gate and drain noise. In contrast with the previous technique, the current amplifiers technique directly provides the two noise sources i_G and i_D physically located at the device terminals [7] and not the *equivalent* voltage/current noise generators V and I.

B. Low frequency noise behaviour

In order to have an exhaustive signature of the low frequency noise behavior of the devices under investigation, we have simultaneously measured at the wafer level not only the input noise current S_{IG} and the output noise current S_{ID} including the cross correlation but also the input noise voltage S_V, input noise current S_I and their correlation. It will be shown that each of these techniques benefits from each other when the origin and the location of the noise sources [7,8] are under consideration.

a. Gate noise current spectral density

In figure 3, we have plotted several gate current spectra for different gate bias when drain source voltage has been kept constant at 0.5 Volts. We observe 1/f like noise that increases with decreasing V_{GS}. We can correlate this increase of S_{IG} with the observed increase of the DC gate current when $|V_{GS}|$ increases. At this stage, the explanation concerning the origin of the excess noise is still on going as more measurements are needed in order to get a deeper insight concerning this behaviour. Similar characteristics have already been observed in AlGaN/GaN HEMT's [12,13]. Nevertheless it can be stated that this gate noise will possibly impact on the design of a low phase noise oscillator.

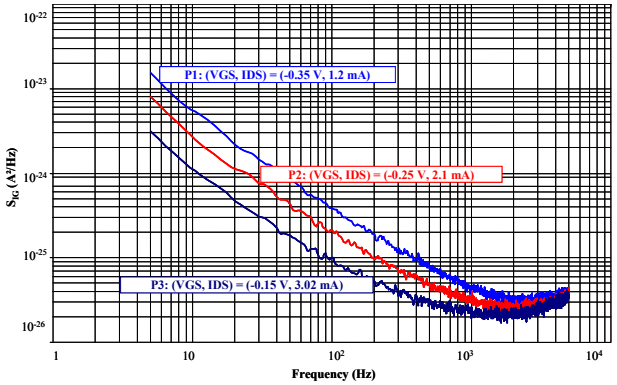

Fig. 3. S_{IG} measured (device 2*50*0.5 µm² at V_{DS}=0.5V).

In figure 4, we have plotted S_{IG} at 10 Hz and V_{DS} = 0.5 V versus I_G : we observe a linear dependence of S_{IG} versus I_G. Additional noise measurements have been carried out in order to get a better insight.

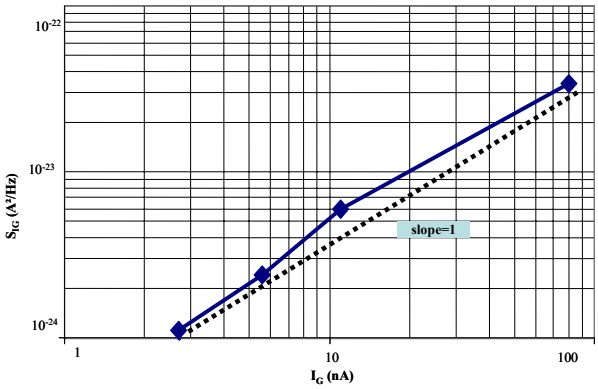

Fig. 4. S_{IG} versus I_G at f = 10 Hz.

Figure 5 displays the frequency dependence of S_{IG} versus the gate length for a device featuring a 50 µm gate width. We observe that LFN gate noise inversely scales with the gate length and hence with the gate surface. Such behaviour is observed in all types of FET devices as long as noise related to surface gate leakage is not pre-eminent. Therefore bulk effects are involved and this statement suggests that 1/f noise at the gate terminal is related to mobility fluctuations or mostly carrier diffusion in the space charge region under the gate [11]. Additionally, the gate current noise strongly increases when the Schottky diode is forward biased, and such an increase of the 1/f noise magnitude can be associated with fluctuations of the Schottky barrier height [12].

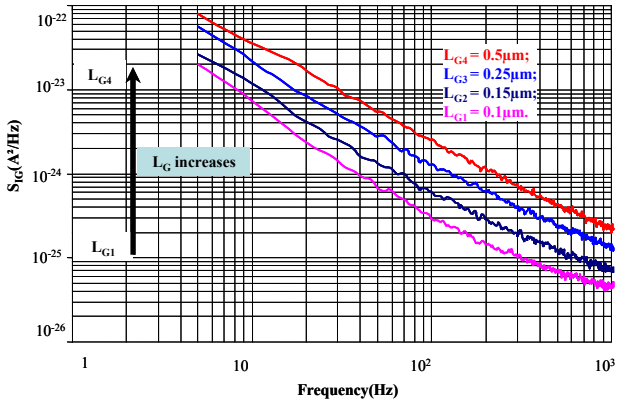

Fig. 5. S_{IG} versus gate length for V_{DS} = 0.5 V and V_{GS} = 0.35 V.

b. Drain noise current spectral density

In figure 6, we have reported noise measurements at the drain terminal versus different I_{DS} and V_{DS} values. Noise spectra indicate that 1/f and generation-recombination noise are superimposed. This important result suggests that the physical mechanisms producing the noise at the gate and at the drain terminal are probably different.

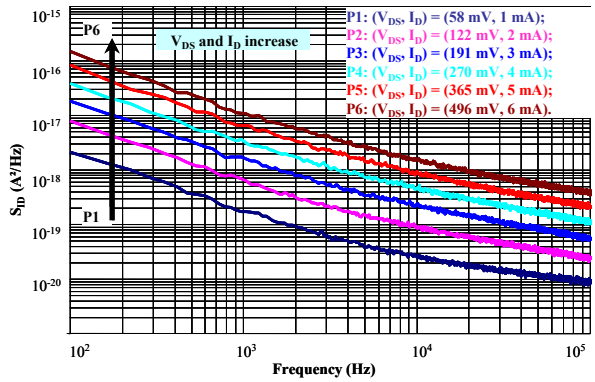

Fig. 6. S_{ID} versus different V_{DS} and at V_{GS} = 0.5 V.

In figure7, we have plotted the drain noise measured at 400 Hz versus the drain current and the results show two different regions. One region, where the noise is varying with I_D^2, corresponds to a noise originating from carrier number fluctuations due to traps while the other region, with a slope equal to 3, shows an additional noise source similar to the one reported in reference [13].

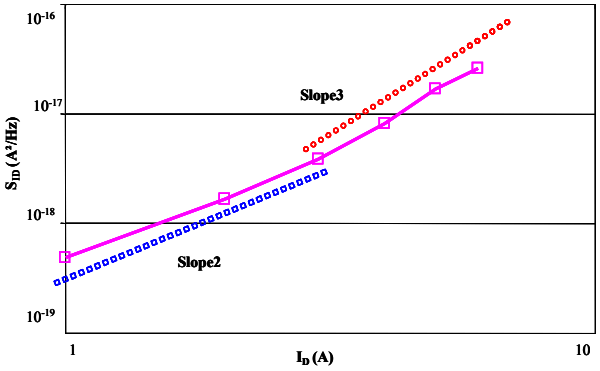

Fig. 7. S_{ID} at 412 Hz versus I_D.

c. Coherence

For all of the bias points investigated, we have observed a coherence γ close to 0 (as an example, figure 8 shows γ versus frequency for V_{DS} = 1.5 V, V_{GS} = -0.2 V, I_D = 1.4 mA and I_G = 68 nA) confirming that the gate and drain noise generators are almost uncorrelated and that the physical mechanisms involved at the gate and drain terminals are different.

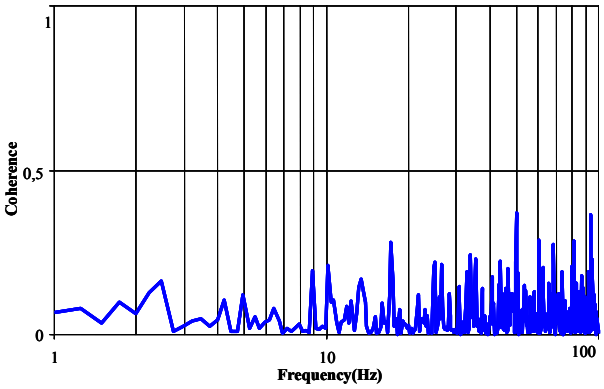

Fig. 8. γ Measurement at V_{DS} = 1.5 V, V_{GS} = -0.2 V, I_D = 1.4 mA and I_G = 68 nA.

C. SiGe MODFET's Phase Noise Behavior

It is understood that low frequency noise is driving the RF phase noise capabilities of a device through a very complicated up-conversion processes. In order to verify this point and to determine which process is primarily involved in the phase noise performances, we have conducted phase noise measurements in an open loop configuration. The measurements have been carried out at 10 GHz for an input power of 0 dBm. Figure 9 presents the residual phase noise measurement versus gate voltage. The results indicate that the gate noise is not playing a strong role in the conversion process since the residual phase noise decreases at V_{GS}=0V as the gate noise is expected to increase. Therefore the drain noise is mostly responsible for the observed device residual phase noise.

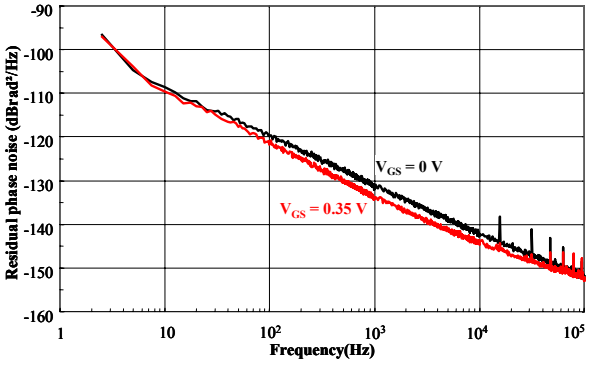

Fig. 9. Residual phase noise at 10 GHz at different V_{GS} (V_{GS}= 0 V and V_{GS}=0.35 V).

IV. CONCLUSION

This paper reports on the low frequency noise characterization of SiGe based n-type MODFETs. In contrast with III-V devices, it has been observed these MODFETs show a non negligible gate noise which scales with the gate leakage current and that can be due to carrier diffusion across the gate space charge. Drain noise has classically been found to originate from number fluctuations in the channel. Moreover gate/drain noise correlation measurements confirm that gate and drain noise originate from different physical mechanisms. Finally, residual phase noise measurements have been performed at 10 GHz and the results let us expect that unconverted drain current fluctuations are mostly responsible for residual phase noise. This result is important for future works dealing with the design of low phase noise oscillator based on these devices.

ACKNOWLEDGEMENTS

The authors wish to acknowledge Dr. T. Hackbarth, Dr. M. Zeuner and Dr. U. König, from Daimler Chrysler Research Center, Ulm in Germany for the supply of the components used in this study.

REFERENCES

[1] A.Coustou, «Conception et caractérisation de circuits intégrés en technologie BiCMOS SiGe pour application de télécommunication en bande X», Thèse de L'Université Paul Sabatier Toulouse 2001, N° 1654.

[2] J.Sadowy «Conception de circuit faible bruit SiGe pour réseaux locaux sans fil en bande C», Thèse de L'Université Paul Sabatier Toulouse 2002, N° 2654.

[3] F. Aniel, N. Zerounian, R. Adde, M. Zeuner, T. Hackbarth, U. König, « Low temperature analysis of 0.25µm T-Gate strained Si/$Si_{0.55}Ge_{0.45}$ n-MODFET's », IEEE Trans. On Electron Devices, July 2000, Vol. 47, pp. 1447-1483.

[4] A.F. Anwar, L. Kuo-Wei, V.P. Kesan, « Noise performance of Si/$Si_{1-x}Ge_x$ FET's » IEEE Trans. On Electron Devices, 1995, Vol 42, pp. 1841-1846.

[5] M. Glük, T. Hackbarth, U. König, A. Haas, G. Hock, E. Kohn, « High Fmax n-type Si/SiGe n-MODFET's », Electronics Letters, February 1997, Vol. 33, pp. 335-337.

[6] U. König, M. Zeuner, G. Höck, T. Hackbarth, M. Glück, T. Ostermann, M. Saxarra, « n and p-type SiGe HFETs and circuits », Solid State Electronics, 1999, Vol. 43, pp. 1383-1388.

[7] L. Bary, M. Borgarino, R. Plana, T. Parra, S.J. Kovaci c, H. Lafontaine, J. Graffeuil**,** « TransimpedanceAmplifie r-Based Full Low-Frequency Noise Characterization Setup for Si/SiGe HBTs », IEEE Trans. On Electron Device*s*, April 2001, Vol. 48, no. 4, pp. 767-773.

[8] M.Borgarino, R. Plana, L. Escotte, S.L. Delage, H. Blanck, , F. Fantini, J. Graffeuil**,** "DC, RF and low frequency noise characterization of C and In/C doped GaInP/GaAsHBT's ", 5th GAAS'97,pp 179-182.

[9] J.A. Garrido, F. Calle, E. Munoz, I. Izpura, J.L. Sanchez-Rojas, R. LI, K.L. Wang, Electronics letters, Vol 34.

[10] S.H. Shawn, P. Valizadeh, D. Pavlidis, « Characterization and analysis of Gate and Drain LFN in AlGaN/GaN HEMTs » Repport of HRL Laboratories, USA. (2001).

[11] T.G.M. Kleinpenning, « Low frequency noise in schottky barrier diodes», Solid-State Electronic, 1979, Vol.22, pp.121-128.

[12] S. T. Hsu, « Low frequency excess noise in metal-silicon schottky barrier diodes», IEEE Trans on Electron Devices, 1970, Vol.17, pp.496-506.

[13] A. Pénarier, S.G. Jarrix, C. Delseny, F. Pascal, J.C. Vildeuil, M. Valenza, D. Rigaud, « Low frequency noise in III-V high-speed devices», IEE Proc. –Circuits Devices Syst, February 2002, Vol. 149, pp.59-67.