Measurements and Simulations of Hot-Carrier Degradation Effects in AlGaAs/GaAs HFETs

A. Mazzanti, G. Verzellesi, A.F. Basile, C. Canali, G. Sozzi*, R. Menozzi*

Università di Modena e Reggio E. and INFM, Dipartimento di Ingegneria dell'Informazione, via Vignolese 905, 41100 Modena, Italy, e-mail: giovanni.verzellesi@unimo.it
* Università di Parma, Dipartimento di Ingegneria dell'Informazione, Parco Area delle Scienze 181A, 43100 Parma, Italy, e-mail: roberto.menozzi@unipr.it

Hot-carrier degradation effects are investigated in AlGaAs/GaAs HFETs by coupling measurements and two-dimensional device simulations. It is shown that only a simultaneous, localised increase of defects at the gate-drain recess surface and channel-buffer interface can thoroughly account for the observed post-stress device behaviour in terms of drain saturation current decrease, reverse gate current increase, gate-lag enhancement.

INTRODUCTION

Understanding the physical mechanisms behind high-field degradation of III-V FETs is essential to improve the reliability of these devices in state-of-the-art microwave power applications. The physical mechanism which is most frequently held responsible for high-field degradation is the hot-carrier-induced generation of interface states at the semiconductor-passivation surface between gate and drain. Electrons trapped by these states and into the passivation would lead to increased surface depletion and, consequently, to drain series resistance increase, drain saturation current (I_{DSS}) and transconductance (g_m) reduction, as well as breakdown walkout. However, a conclusive validation of this degradation mechanism, showing that it can provide consistent explanation for the manifold consequences of hot-electron stress, is still lacking.

In this paper, we show how comparison of measurements and device-simulation outputs can provide insight about the main degradation effects observed in AlGaAs/GaAs HFETs and contribute to the comprehension of the underlying physical mechanisms.

SAMPLES AND NUMERICAL MODEL

Devices adopted for this study are double-recess power HFETs fabricated at Alenia Marconi Systems with the following bottom-up structure: GaAs SI substrate; AlGaAs/GaAs multilayer buffer; 75 nm thick n-GaAs channel, Si-doped at $4x10^{17}cm^{-3}$; $Al_{0.25}Ga_{0.75}As$ barrier layer, Si-doped at $2x10^{17}cm^{-3}$, 30-nm thick under the gate; n^+-GaAs cap for low-resistance ohmic contacts. Gate width and length are 200 μm and 0.25 μm, respectively. Typical electrical parameters measured in these devices are I_{DSS}≈200 mA/mm, g_m≈150 mS/mm, pinch-off voltage V_T≈-2 V, off-state drain-source breakdown voltage (measured at I_G=-1 mA/mm) BV_{DS}^{OFF}=17 V, off-state drain-gate voltage BV_{DG}^{OFF}=19-20 V. At 10 GHz and 1-dB compression, the typical power density and gain are 0.6 W/mm and 9.6 dB, respectively. Additional details about device fabrication technology can be found in (1).

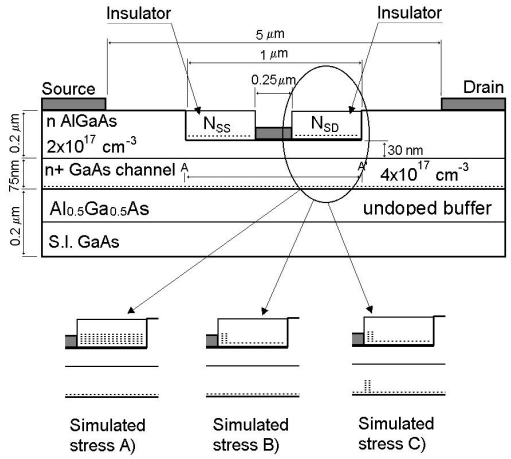

Figure 1: Sketch of the simulation domain (not to scale).

Two-dimensional device simulations were performed with the program DESSIS-ISE (2). The hydrodynamic transport model was adopted for electrons, whereas holes were treated with the computationally more efficient drift-diffusion model. The electron-initiated impact-ionization (i.i.) rate was expressed as a function of the electron energy through the so-called effective-carrier-temperature model (2), allowing non-local i.i. effects to

be accounted for. The simulation domain is sketched in Fig. 1. In order to account for process damage in the as-fabricated devices, a density of $2x10^{12}$ cm^{-2} acceptor-like surface states was defined at the $Al_{0.25}Ga_{0.75}As$ recess surfaces between gate and drain and between gate and source. Based on g_m frequency dispersion and DLTS results, we set the energy of these states at 0.36 eV above the top of valence band (E_V), and their apparent cross-section at $2x10^{-17}$ cm^{-2} both for electrons and holes (3). A negative fixed charge density of $6x10^{11}$ cm^{-2} was instead placed at the $GaAs/Al_{0.5}Ga_{0.5}As$ interface in order to account for electrons trapped in the buffer and substrate and to achieve a good fit of the measured V_T.

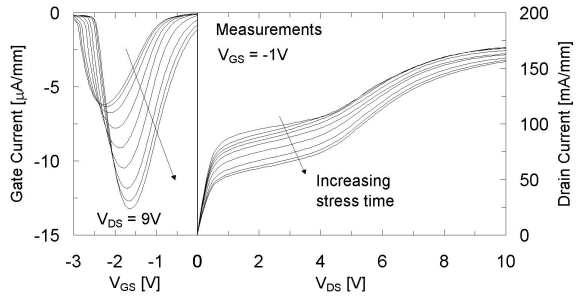

Figure 2: Experimental I_D-V_{DS} and I_G-V_{GS} characteristics at increasing stress time.

RESULTS

The HFETs underwent room temperature DC hot-electron accelerated stress under several different bias conditions (1). Fig. 2 shows how hot-carrier stress impacts the I_D-V_{DS} and the bell-shaped I_G-V_{GS} curves. The stress conditions are I_G=-0.5 mA/mm, I_D=0.5 mA/mm, corresponding to an initial V_{DG} = 20.3 V. As can be seen, I_{DSS} decreases at increasing stress time (it reaches a 30% degradation in about 10 hours under the applied stress conditions). At the same time, the $|I_G|$ peak increases. As widely known, the bell-shaped I_G vs. V_{GS} curve originates from the opposing trends of current density and electron temperature versus V_{GS}: while the current increases with V_{GS}, the electrons cool down due to field relaxation; consequently, the impact ionisation rate and the gate current, which depend on both the electron current density and energy, peak around V_{GS} ranging from -2 V to -1.5 V. Other degradation effects always observed in these devices are a reduction of g_m, an increase in the drain access resistance (measured by an end-resistance method) and the walkout of the off-state breakdown. An extensive description of accelerated-stress results can be found in (1).

Device simulations are able to reproduce the experimentally observed hot-electron stress effects, provided that suitable distributions of surface states/fixed charges are accounted for at the barrier-passivation and channel-buffer interfaces in gate-drain access region. More specifically, simulation results can be summarized as follows.

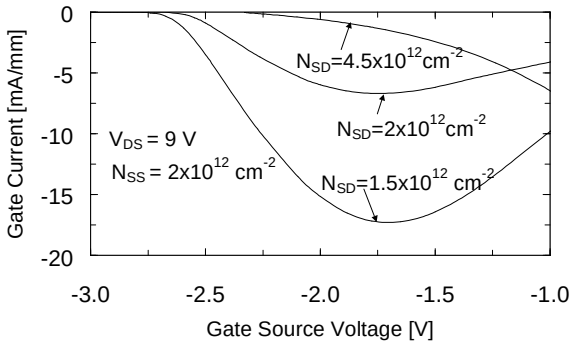

Figure 3: Gate current versus gate-source voltage curves for increasing uniform surface damage (simulated stress A).

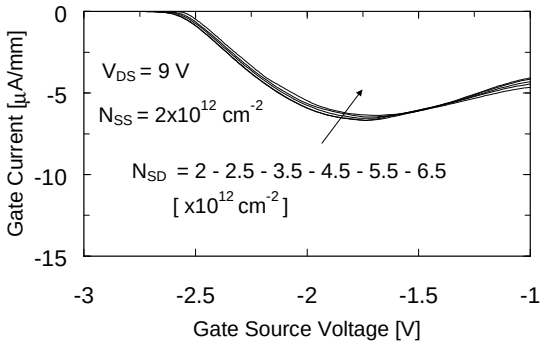

Figure 4: Gate current versus gate-source voltage for increasing localised surface damage (simulated stress B).

The surface hot-carrier-induced damage must be concentrated into a narrow (≈70 nm) portion of the gate-drain recess adjacent to the gate, otherwise the bell-shaped $I_G(V_{GS})$ curve can not be reproduced by simulations with high surface-state densities at the gate-drain surface (N_{SD}). As a matter of fact, if a high N_{SD} is uniformly distributed throughout the gate-drain recess surface (**simulated stress A**, Fig. 1), the electric field peak shifts laterally into the drain access region, resulting in reduced V_{GS} control on peak electric field and impact-ionisation rate. As a result, the reverse gate current become a monotonic function of V_{GS}, i.e. the $I_G(V_{GS})$ bell curve is not reproduced by simulations (see Fig. 3), whereas, experimentally, it is still observed even in the most degraded devices (see Fig. 2). When the increase of N_{SD} simulating the hot-carrier damage is confined to a narrow (70 nm) portion of the gate-drain recess adjacent to the gate (**simulated stress B**, Fig. 1), the I_G bell

survives even at the higher N_{SD} value considered. However, the effect of the simulated stress on the I_G versus V_{GS} curves is weak and opposite in sign to the measured one (see Fig. 4).

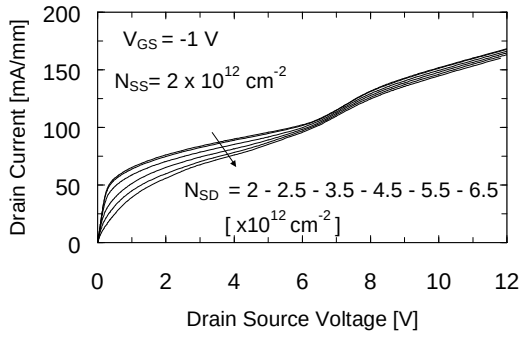

Figure 5: Simulated output characteristics for increasing localised damage at the gate-drain surface and channel-buffer interface (simulated stress C).

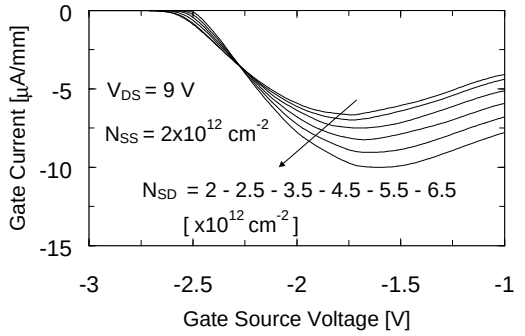

Figure 6: Simulated I_G vs V_{GS} curves for increasing localised damage at the gate-drain surface and channel-buffer interface (simulated stress C).

The increase in the localised surface damage must be accompanied by a corresponding increase of negative charge density at the channel/buffer interface, if one wants to match simultaneously the I_D degradation and the $|I_G|$ peak increase observed experimentally at increasing hot-electron stress. Figs. 5 and 6 show simulation results obtained by increasing N_{SD} from 2x10^{12} cm^{-2} to 6.5 x10^{12} cm^{-2} in a 70-nm-wide surface region on the drain side of the gate, but at the same time raising the fixed negative charge at the bottom channel interface by 10% of the surface increase of N_{SD}, in a 100-nm segment between gate and drain (**simulated stress C,** Fig. 1). This time, an I_D reduction similar to the measured ones were simulated (Fig. 5), as well as the increase of the bell curve peak (Fig. 6). Inspection of the simulation outputs shows that this simulated stress results in an increase of the peak electron temperature, only partially compensated by a reduction of the channel current density: the net result is a significant enhancement of the impact ionisation rate, hence the increase of I_G of Fig. 6.

In agreement with experimental results (Fig. 2), simulations shown in Fig. 5 exhibit a kink at V_{DS}≈6 V. Simulations allow the physical origin of the kink to be elucidated. While for V_{DS}<6 V nearly all of the states on the source side are occupied by electrons, at the V_{DS} value (about 6 V) for which channel impact ionisation becomes significant, surface deep acceptors get partly discharged due to hole capture, thus reducing the depletion region under the ungated surface, see Fig. 7. This in turn leads to I_D increase, hence the kink. As already observed in (4), the kink is present in the simulated output characteristics only if both i.i. and surface deep levels are accounted for (see Fig. 8).

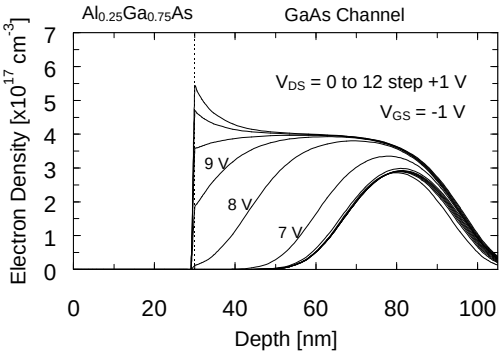

Figure 7: Electron density along a vertical cut inside the source access region for different V_{DS} for an as-fabricated device (N_{SD}=N_{SS}=2x10^{12} cm^{-2}).

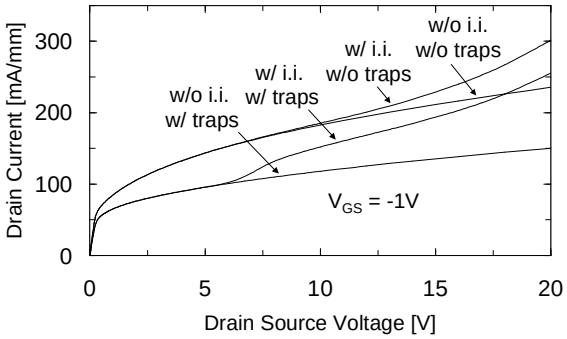

Figure 8: Simulated output characteristics with and without impact ionisation and with and without surface states (N_{SD}=N_{SS}=2x10^{12} cm^{-2} when considered).

Gate-lag waveforms of differently degraded devices can be accurately simulated by varying the localised surface-state density N_{SD} in a relatively narrow range (from 2.5 × 10^{12} cm^{-2} to about 3 ×10^{12} cm^{-2}), see Fig. 9. In agreement

with (5), we found that the surface states act as hole traps during the switching transients. The turn-off transient is in particular governed by hole emission, resulting in surface negative-trapped-charge increase (see Fig. 10), this in turn leading to conductive channel narrowing and I_D decrease (see Fig. 9). It is worth mentioning that if surface traps were instead placed at 0.36 eV below the bottom of the conduction band (instead of being assumed at $E_t=E_V+0.36$), no dynamic effect would appear in the simulated $I_D(t)$ transient following a V_{GS} step, in contrast to what experimentally observed (thus ruling out this possibility). Actually, due to the negative trapped charge, bands are actually upward bent at the ungated surface, so that only the occupancy of trap levels sufficiently close to E_V can be appreciably modulated by the surface electric potential.

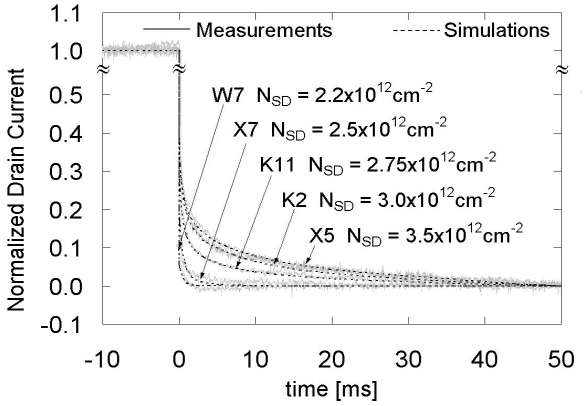

Figure 9: Experimental and simulated (simulated stress C) normalised I_D transients following a reverse-bias V_{GS} step (from 0 to –0.5V) in differently degraded devices.

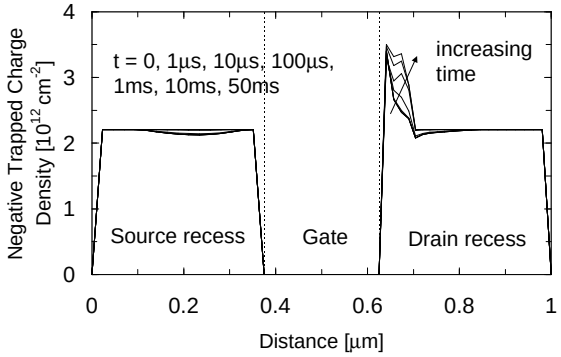

Figure 10: Negative-trapped-charge dynamics during the transient following a reverse-bias V_{GS} step (from 0 to –0.5V) for $N_{SD}=3.5x10^{12}$ cm^{-2} (simulated stress C).

CONCLUSIONS

We have presented experimental and simulation results showing that only a simultaneous, localised increase of the defect density at the gate-drain recess surface and channel-buffer interface can thoroughly account for the hot-electron degradation modes observed experimentally in AlGaAs-GaAs HFETs, including drain saturation current degradation, reverse gate-current increase and gate-lag enhancement. Simulations also allow the physical origin of the kink to be elucidated, attributing it to the discharge of surface deep acceptors due to the capture of excess holes generated by impact ionisation.

ACKNOWLEDGEMENT

The authors wish to thank Dr. A. Cetronio e Dr. C. Lanzieri (Alenia Marconi Systems SpA, Rome, Italy) for providing the devices used for this work. Fruitful discussions with Prof. E. Zanoni and Prof. G. Meneghesso (University of Padova, Italy) are also acknowledged.

REFERENCES

(1) D. Dieci, G. Sozzi, R. Menozzi, E. Tediosi, C. Lanzieri, and C. Canali, "Electric-field-related reliability of AlGaAs/GaAs power HFETs: bias dependence and correlation with breakdown", *IEEE Trans. Electr. Dev.*, vol. 48(9), pp. 1929-1937, Sept. 2001.

(2) DESSIS 6.0 Reference Manual, ISE Integrated Systems Engineering AG, 1999.

(3) D. Dieci, R. Menozzi, C. Lanzieri, L. Polenta, C. Canali, "Hot electron effects on $Al_{0.25}Ga_{0.75}As$/GaAs power HFET's under off-state and on-state electrical stress conditions", *IEEE Trans. Electr. Dev.*, vol. 47(2), pp. 261-268, Feb. 2000.

(4) T. Suemitsu, T. Enoki, N. Sano, M. Tomizawa, Y. Ishii, "An analysis of the kink phenomena in InAlAs/InGaAs HEMT's using two-dimensional device simulation", IEEE Trans. Electr. Dev., vol. 45(12), pp. 2390-2399, Dec. 1998.

(5) K. Horio, T. Yamada, "Two-Dimensional Analysis of Surface-State Effects on Turn-On Characteristics in GaAs MESFETs," *IEEE Transactions on Electron Devices*, vol. 46, no. 4, 1999, pp. 648-655.