W-Band Low-Loss Wafer-Scale Package for RF MEMS

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***Abstract*— This paper reports on the design and fabrication of a wafer-scale package for RF MEMS devices at W-band. Coplanar waveguide (CPW) lines on a high resistivity silicon wafer are covered with another silicon wafer using gold-to-gold thermo-compression bonding. Oxide is used as a dielectric inter-layer for CPW feedthroughs underneath the gold sealing ring. A 130 μm high cavity is etched in the cap wafer to remove an impact of capping wafer on CPW lines or RF MEMS components. The designed feedthrough has an insertion loss of 0.19−0.26 dB at 75−110 GHz with a return loss of < -20 dB (per transition). The gold sealing ring is connected to the CPW ground to eliminate any parasitic ring effect of the gold sealing ring. The whole package has a measured insertion loss of 0.6−0.8 dB and return loss of < -20 dB at 75−110 GHz.**

I. Introduction

Numerous RF MEMS devices such as switches, varactors, and resonators have been demonstrated with outstanding RF performance [1] . Several low loss MEMS devices have been demonstrated at W-band. However, these low loss devices can only be as good as their packaging can allow. The RF MEMS devices must be encapsulated in a stable environment to protect their movable parts. There have been several attempts on wafer-scale packages to provide a hermetic sealed cavity using various wafer bonding techniques. Schöbel et al. used a glass frit bonding with 0.25−0.5 dB insertion loss of a CPW feedthrough at W-band [2]. Margomenos et al. used gold thermo-compression bonding with 0.06 dB insertion loss of a hermetic via-hole transition up to 60 GHz [3]. At lower frequecy, Jourdain et al. reported 0.09−0.15 dB insertion loss at 2 GHz with a solder (SnPb) bonding [4]. Radant MEMS presented a DC−40 GHz packaged switch with a return loss of less than −20 dB using glass frit bonding [5]. We also have demonstrated a wafer-scale package at DC−50 GHz using thermo-compression bonding with an insertion loss of less than 0.1 dB [6]. In this paper, we follow the previous CPW-based approach with an oxide interlayer for W-band applications, and show that grounding of the metal sealing ring removes any parasitic resonance. If a surface-mount package is needed, the via-holes can be placed *outside* of the hermetic package using a standard low-cost process.

II. Design

The package is realized using gold-to-gold thermo-compression bonding of two silicon wafers as shown in Fig. 1. On the bottom wafer, the 25/50/25 μm CPW line is designed to achieve 50 Ω transmission line. 1000 Ω-cm high resistivity silicon wafers are used for the bottom and cap wafers to decrease the CPW line loss. A 130 μm cavity is etched in the cap wafer to remove the impact of placing a silicon cap in near proximity of the CPW lines or RF MEMS components. Therefore, the CPW lines or RF MEMS components do not need to be redesigned for use inside the package. The gold ring over oxide inter-layer provides a bonding area and sealing for the hermetic package. The gold ring is connected to the CPW ground, and this grounding removes any parasitic ring effects.

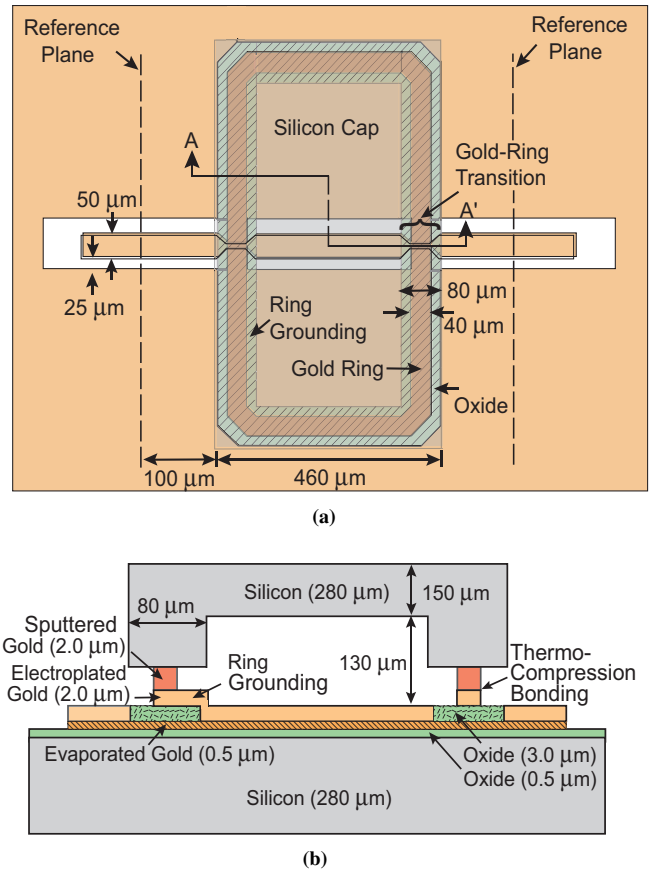

Fig. 1. Top view (a) and AA' cross section (b) of the proposed package scheme with a packaged CPW transmission line.

Underneath the gold ring, the width of the CPW center conductor is narrowed down to 10 μm to compensate for the capacitive loading of the gold ring (see Fig. 1, gold-ring transition). The narrowed capacitive line ($l = 40$ μm) is also matched by the inductive tapering in the CPW line. Fig. 2 shows the simulated insertion loss and return loss using

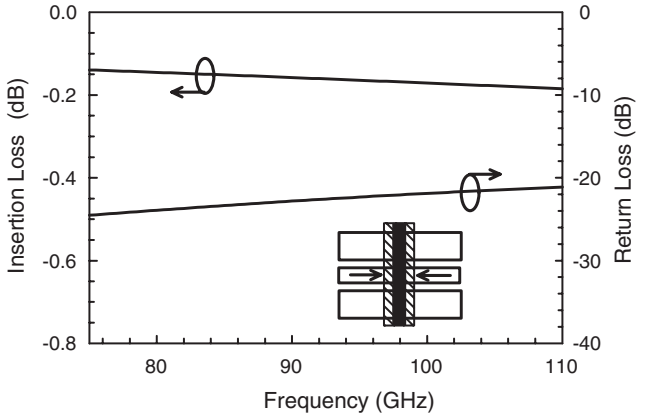

Fig. 2. Simulated insertion loss and return loss of the gold-ring transition using Sonnet

Sonnet[1] simulator. The simulated return loss of the transition is lower than -21 dB at W-band. The simulated loss of the transition is $0.14-0.18$ dB at W-band due to the thin ($t = 0.5$ μm) and narrow ($w = 10$ μm) CPW center conductor underneath the gold ring.

III. Fabrication

The CPW line is fabricated on a 280 μm thick silicon substrate. The first step is a lift-off process of Ti/Au/Ti 300/4400/300 Å which patterns the CPW line and the thin feedthrough layer. This feedthrough must be thin to make a relatively planar bonding surface. The next step is a PECVD deposition of 3 μm oxide (SiO_2), which is patterned using an RIE process. This oxide layer provides the dielectric interlayer between the CPW line and the gold sealing ring. Then, a 300/1000/300 Å Ti/Au/Ti seed layer is evaporated and then the 2 μm thick CPW line and sealing ring are electroplated. On a separate 280 μm thick cap wafer, a 2 μm of Au layer is sputtered first, and the sealing ring is patterned with wet etching. The next step is a lift-off process of align keys on the backside of the cap wafer for the future bonding process. Then, a 1000 Å of Al layer is sputtered and patterned to provide a DRIE mask of the 130 μm high package cavity. Before this cavity is etched, opening holes for the CPW probe measurement is etched first about 160 μm using photo resist mask. The final step is the gold-to-gold thermo-compression bonding of the two silicon wafers. The wafers are heated to 340°C and a pressure of 1000 $\mathrm{lbf/in^2}$ is applied for an hour. This bonding technique has shown proven high reliability hermetic sealing [3], [7]. The hermeticity of these particular packages have not been tested.

[1]Sonnet, ver. 9.52, Sonnet Software Inc., Syracuse, NY, 1986-2003.

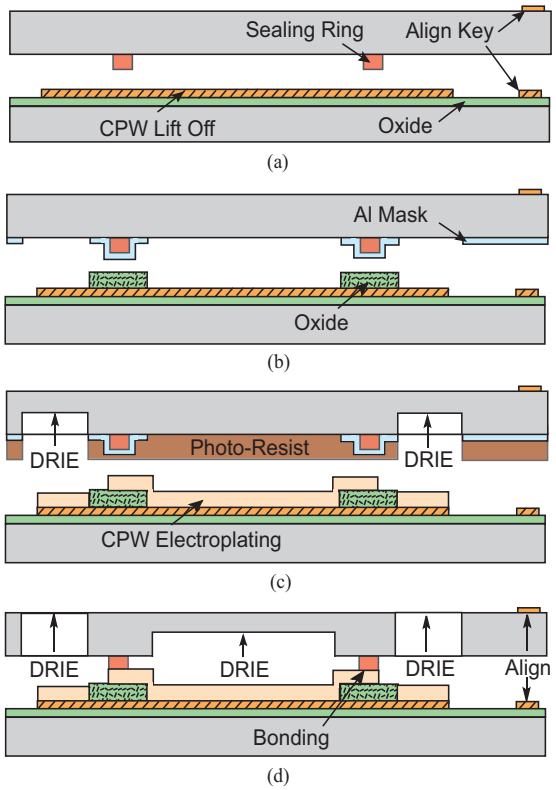

Fig. 3. Fabrication process flow of the package

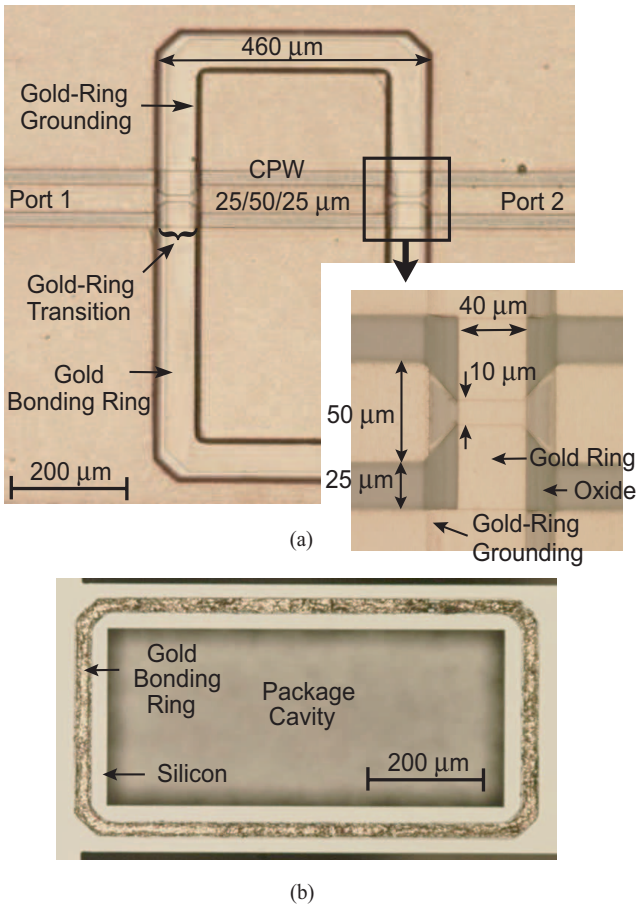

Fig. 4. Picture of the bottom wafer (a) with a magnified gold-ring transition, and the cap wafer (b).

IV. Simulation and Measurement

Table I summarizes the simulated and measured RF characteristics of the CPW line and the gold-ring transition. S-parameters of the CPW lines are measured on an HP 8510C Network Analyzer, using a TRL calibration method to de-embed the probe-to-wafer transition and establish reference

TABLE I
SUMMARY OF MEASURED AND SIMULATED CHARACTERISITCS OF CPW LINE AND GOLD-RING TRANSITION

	Freq.	Sim/Meas	Characteristics
CPW w/ & w/o Si Cap	90 GHz	Sim.*	Zo=51, α=310 dB/m, ε_{eff}=6.3
		Meas.	Zo=49, α=210 dB/m, ε_{eff}=5.6
Gold-Ring Transition	75 GHz	Sim.*	I.L.= 0.14 dB, R.L.= -25dB
		Meas.	Added I.L. = 0.20 dB
	90 GHz	Sim.*	I.L.= 0.16 dB, R.L.= -23dB
		Meas.	Added I.L. = 0.23 dB
	110 GHz	Sim.*	I.L.= 0.18 dB, R.L.= -21dB
		Meas.	Added I.L. = 0.26 dB

*ε_{si} = 11.9, σ_{si} = 0.1 S/m, tanδ_{si} = 0.003, ε_{oxide} = 3.8, and σ_{gold} = 3x10^7 S/m

planes as shown in Fig. 1. The CPW characteristics are measured using many 1,000 μm and 2,000 μm long CPW lines with and without the silicon cap. The silicon cap, with 130 μm high cavity, has no apparent impact on the CPW characteristics. The measured loss and impedance of CPW line (25/50/25 μm) are lower than the Sonnet simulation because the oxide layer between CPW center conductor and ground is etched. The measured insertion loss of the packaged CPW lines and CPW lines that are not packaged are shown in Fig. 5. The loss due to the gold-ring transition can be estimated by their difference. For clearance, the loss in both cases are least-squares fitted to $b + a\sqrt{freq.}$ functions since the loss in CPW lines are mainly ohmic and have a known frequency dependance [8]. The measured and simulated loss per transition is summarized in Table I at 75, 90, and 110 GHz. The measured packaged line loss is about 0.07 dB higher than the Sonnet simulation. This is possibly due to the oxide layer which is charged under the CPW line. This oxide layer attracts minority carriers of the semiconductor and results in a localized low resistivity inversion layer at the silicon surface [9]. Therefore, the loss of the CPW line under gold-ring transition increases.

Fig. 6 presents the HFSS[2] simulated and measured insertion loss and return loss of the CPW line. For the HFSS simulation,

[2]HFSS, ver. 9.2, Ansoft Corporation, Pittsburgh, PA, 1984-2004.

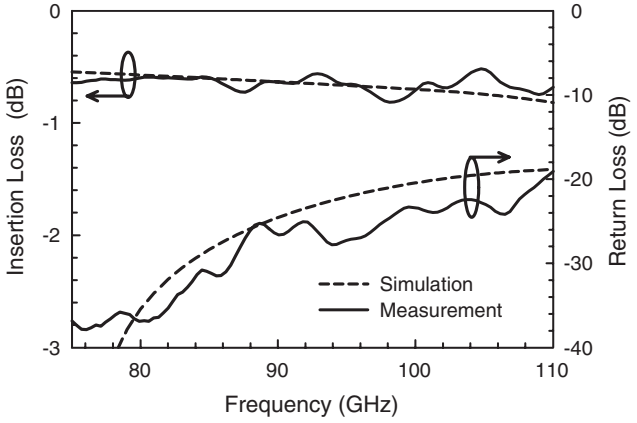

Fig. 6. Measured and simulated insertion loss and return loss of a package.

the conductivity of gold feedthrough is lowered to compensate the difference between the simulated and measured transition loss in Table I. The return loss of the package is mainly determined by the gold-ring transition and is better than -20 dB. Fig. 7 presents the input/output isolation of the packaged CPW line with a 60 μm-long gap in the center conductor. This represents the case of an RF MEMS switch in the up-state position. Due to the return loss of the gold-ring transitions, the isolation of the packaged CPW line is better than the isolation of the CPW line which is not packaged if there is no severe leakage by the package. The measured isolation agrees well with the simulation and does not show any severe leakage. The reason is that the grounded gold ring does not allow leakage between the input and output transitions.

V. CONCLUSION

This paper demonstrates a straight-forward design for W-band transitions suitable for RF MEMS packages. The loss per transition is less than 0.26 dB up to 110 GHz. The transition loss was checked with the difference between the not packaged CPW line loss and the packaged CPW line loss. The package

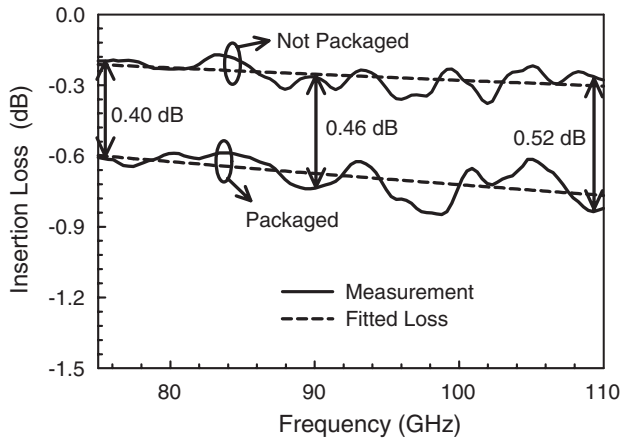

Fig. 5. Measured and fitted insertion loss of the CPW line and the packaged CPW line. The added loss includes the effects of two transitions.

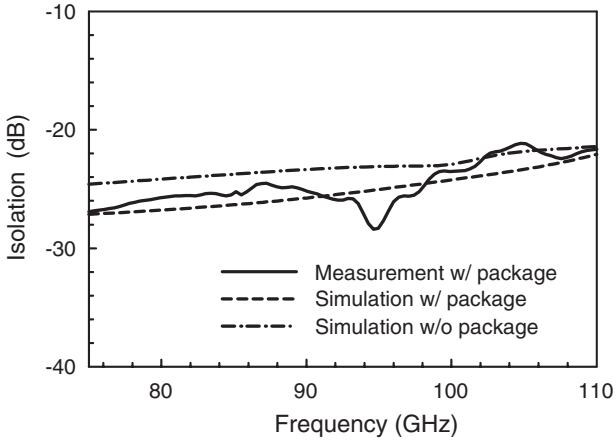

Fig. 7. Measured and simulated isolation of a 60 μm gap in the CPW line and the packaged CPW line.

has a measured return loss of < -20 dB at $75-110$ GHz. This package is also suitable for amplifiers, mixers, and any GaAs or SiGe integrated circuit and is not limited to RF MEMS devices.

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