# Analysis of Device Scaling towards the Performance Enhancement of Si-MOSFET RF Amplifiers

Padmanava Sen, Nuttapong Srirattana, Arvind Raghavan* and Joy Laskar

Georgia Electronic Design Center, School of ECE, Georgia Inst. of Technology, Atlanta, GA 30308, USA
Email: psen@ece.gatech.edu

*Quellan Co., Atlanta, GA 30308, USA

***Abstract* — This paper explains the importance of device size and dc bias conditions for the gain and linearity performance enhancement of silicon based RF amplifiers. In this work, the existence of an optimum device size for maximum gain, for the given bias conditions and load impedances is explained by determining the small-signal gain parameters for a common source amplifier as functions of the device size and dc bias conditions. Also, the change of optimum device size with the bias conditions and the load impedances is analyzed. A Taylor series expansion is used to determine the extent of weak nonlinearity for different device sizes. IP3 measurements suggest that the distortion is minimum for a particular device size. The analysis presented in this paper enables the optimization of the performance of Si-MOSFET based RF amplifiers. The frequency chosen for analysis is 2.4GHz.**

***Index Terms* — Gain, linearity, RF amplifiers, small signal, device size.**

## I. Introduction

In recent years, there has been a great deal of research aimed at realizing a low cost, low power and compact transceiver front-end in the commercial RF bands. RF CMOS technology offers great promise in achieving this end. However, careful and optimized design of RF CMOS circuits is essential to realize this objective. The variation of the gain and linearity characteristics of a Si-MOSFET with device periphery, load impedance and bias conditions, is commonly observed. Though the gain as well as noise optimization for design of LNA ([1], [2]) and linearity analysis for RF applications ([3], [4]) are already studied, there is a need for a systematic analysis and understanding of these phenomena in order to be able to maximize circuit performance. This paper addresses that need. The analysis is mainly aimed to solve the problem of choice of the driver stage device size to get the required gain. Also, the extent of linearity/non-linearity involved in the pre-amplifier or the driver stage of a power amplifier is analyzed. Still, the methodologies are applicable to the design of other RF CMOS amplifiers, such as low-noise amplifiers. The linearity of a single stage amplifier for different device sizes is studied assuming the device behavior in a weakly nonlinear domain, so that Taylor series expansion can be applied. The third order intercept points are measured to determine the third order trans-conductance parameters for different device sizes. All the devices used for analysis are thick gate oxide NMOS devices (channel length=0.4 μm, keeping in view of power applications), fabricated in a 0.18μm CMOS process.

## II. Analysis of Gain variations

A high gain, with low distortion, is always desirable in a linear amplifier. However, the gain of an amplifier does not keep increasing with device size. There exists an optimum device size for a certain DC and external matching condition, for which the gain is maximum. A simplified model (shown in Fig 1) is used for the purpose of this analysis. For the frequency band of interest (the 2.4 GHz ISM band), the capacitive effects are more pronounced than the intrinsic resistances. The considerable simplification in obtaining closed-form analytical equations afforded by this simple model warrants the slight loss of accuracy due to the omission of these parameters as shown in Fig. 2(a) for the gain parameter $S_{21}$.

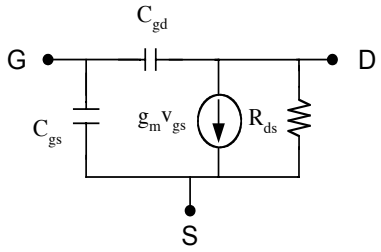



Fig. 1. The Simplified Model for MOSFET

From the model shown in Fig 1, the expression of $S_{21}$ for a device width W is given by;

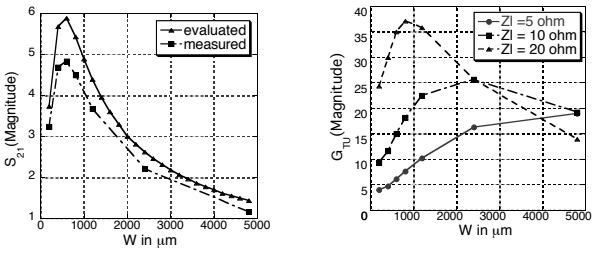
$$S_{21} = \left[ \frac{W(-2c + 2j\omega b)Z_0}{1 + W\{d + j\omega(a+2b)\}Z_0 + W^2\{-ab\omega^2 + \omega(bc+da+bd)\}Z_0^2} \right] \quad (1)$$

The device parameters $g_m$, $g_{ds}$, $C_{gs}$ and $C_{gd}$ increase linearly with the device size and the slopes for the linear variations with W are defined as a, b, c and d respectively. From Appendix I, these values (extracted with a more elaborate model) are 210 mS/mm, 5.9 mS/mm, 1.25 pF/mm, and 0.3 pF/mm respectively. From (1), it is evident that $S_{21}$ is not a linear function of the device size and it reaches a maximum for a certain device size. The extraction algorithm in [5] is used in conjunction with the following procedure to obtain this optimum device size: (i) Devices with a large variations of sizes are fabricated; (ii) From measurement results, the constants a, b, c, d are determined assuming the scalability of the device model in the region of operation; (iii) For the intrinsic model, the value of required gain parameter is plotted with device size; (iv) From the continuous curve, the optimum device size is determined. The procedure can also be used for complex intrinsic models. The variation of $S_{21}$ with device size ($V_{gs}$=1.2 V, $V_{ds}$=2.4 V) is shown in Fig 2(a), which support the consistent nature of variations for measured and evaluated (from analysis and extraction) results.

The most important gain parameter for a circuit is the transducer gain, which is a function of load impedance, matching conditions and two port parameters of the device. The unilateral transducer gain ($G_{TU}$) is determined for different load impedances for conjugate match in the source side. The required equations for determining the transducer gain as a function of width of the device are given below. The measured transducer gains for different load impedances are shown in Fig 2(b).

$$G_{TU} = \frac{|S_{21}|^2\left(1-|\Gamma_S|^2\right)\left(1-|\Gamma_L|^2\right)}{|1-S_{11}\Gamma_S|^2|1-S_{22}\Gamma_L|^2} \qquad (2)$$

where, $\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$, $\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$, $\Gamma_S = \Gamma_{in}^*$




(a) (b)

Fig. 2. (a) The variation of $S_{21}$ with device size, (b) The transducer gain for different load impedances (dc conditions: $V_{gs}$=1.2 V, $V_{ds}$=2.4 V).

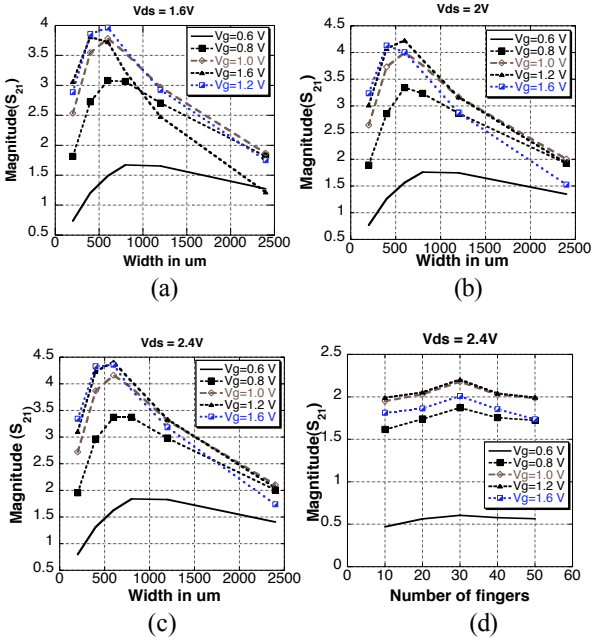
### *Variations with DC conditions:*

The optimum device size is a function of the dc bias conditions because the device intrinsic parameters are also dependent on the gate and drain voltages. Since RF amplifiers typically operate in the saturation regime the expressions of $g_m$ and $g_{ds}$ are given by:

$$gm = \left[\frac{kW}{2L}\frac{(Vgs - V_T)(2+\theta(2-x)(Vgs-V_T)^x)(1+\lambda Vds)}{1+\theta(Vgs-VT)^x}\right]$$
$$gds = \left[\frac{kW}{2L}\frac{(Vgs-V_T)^2(1+\lambda Vds)}{1+\theta(Vgs-V_T)^x}\right] \qquad (3)$$

Where, $\lambda$ is channel length modulation coefficient, $\theta$ and x are velocity saturation scattering parameters. For lower values of $(V_{gs} - V_T)$ the effects of $\theta$ and x can be neglected. But for higher currents and smaller channel lengths, their effects may be significant.

The device capacitances do not change much with the voltage bias as far as the region of operation remains the same. The gain increases with more dc current consumption as $g_m$ increases with $I_D$. But, the optimum device size will not be the same for different bias conditions. The device size for maximum gain ($S_{21}$) decreases with increase of gate to source voltage (for $V_{ds}$=1.6,2,2.4 V) as shown in Fig. 3(a)-3(c). The variation for the same size of device with different number of fingers is shown in Fig. 3(d). The fabricated MOSFET devices with the de-embedding structures are shown in Fig. 4.




(a) (b) (c) (d)

Fig. 3. The $S_{21}$ variation with different gate bias at frequency 2.4GHz for (a) $V_{ds}$=1.6 V, (b) $V_{ds}$=2.0 V, (c) $V_{ds}$=2.4V with gate width variation & (d) $V_{ds}$=2.4 V varying the number of fingers for a 2400 μm device.

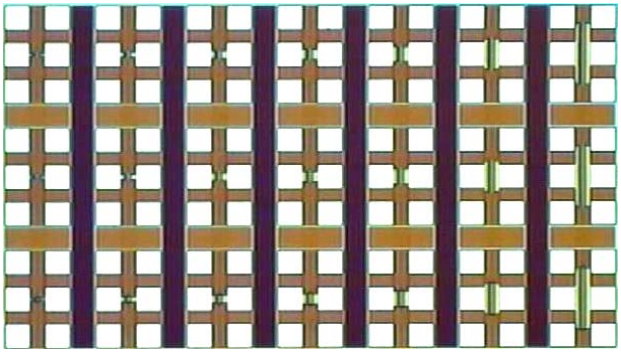


Fig. 4. The devices fabricated

## III. Linearity Variations

Linearity is another parameter that cannot be neglected while designing an amplifier. The linearity requirements of an amplifier mainly depend on the application. The gain stages of a power amplifier should have very good linearity for the power stage to work properly. If the amplifier is weakly non-linear, Taylor series can be applied[6]. The instantaneous drain current as a function of $g_m$ and $g_{ds}$ is given by:

$$i_{ds}(v_{ds}\ ,\ v_{gs}) = I_{ds}(V_{gs},V_{ds}) + g_m v_{gs} + g_{ds} v_{ds} + g_{m2} v_{gs}^2 + g_{md} v_{gs}\ v_{ds} + g_{d2} v_{ds}^2 + g_{m3} v_{gs}^3 + \ldots\ldots\ldots \quad (4)$$

From the above expression, the value of third order interception point (IP3) can be approximated below with the assumption that $g_{ds}$ non-linearity with respect to $g_m$ nonlinearity can be neglected.

$$IP3 = \sqrt{\frac{4g_m}{3g_{m3}}} \quad (5)$$

The IP3 and third order trans-conductance values (for both load and source impedance equal to 50 ohms) are shown in Fig. 5. The IP3 values changes with the power level as the gain saturates and as a result the simple extrapolation gives erroneous expression at higher power levels. The values plotted in Fig. 5 are measured at low power level to get a more accurate expression of $g_{m3}$. The IP3 values are measured using Maury load-pull systems at 2.4 GHz. There is always a certain device size, which exhibits best linearity performance. Using equation (5), the variation of $g_{m3}$ is determined and it is not linear with the device size, as $g_m$ is linear with the device size. From Fig 5, 800μm x 0.4μm is the most linear device among the seven devices chosen for $V_{ds}$ =2.4 V and $V_{gs}$ =1.2 V at 2.4 GHz.

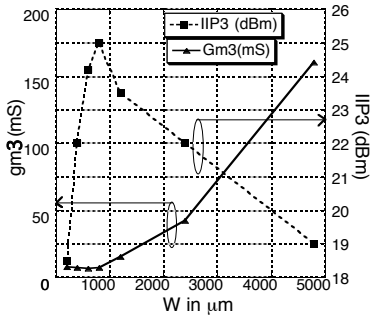



Fig. 5. The third-order trans-conductance and intercept points (dc conditions: $V_{gs}$=1.2 V, $V_{ds}$=2.4 V)

## IV. Discussion

In this work, small signal behavior of a MOSFET is analyzed to optimize the design of a CMOS RF amplifier for gain and linearity. While the optimization conditions for a large-signal non-linear amplifier, such as the output stage of a power amplifier, are difficult to arrive at by pure analytical equations, the techniques derived in the paper offer valuable insights into the behavior of these devices and enable the designer to predict the trends in gain and linearity under large-signal operation. The transducer gain of an amplifier decreases with the input signal level for class A/AB operation, though the gain can be extracted from S-parameters upto a certain input power level for a linear amplifier. The power output and efficiencies for large signal operation can only be extracted from load-pull measurements. As the large signal gain parameters and matching conditions cannot be determined from S-parameters. Those parameters for the final stage of a power amplifier can be determined only from measurements. Also from Fig. 2(b), it is evident that for high power operation (low load impedance), a large device is always preferred for required gain as well as reliability. In case of a power amplifier- if it consists of three stages, the first stage device size should be chosen looking at the matching and gain requirement, the second stage device size should be optimized for a good gain as well as linearity. The final stage device size is mainly chosen for reliability, efficiency and power handling capability. The class of operation has to be chosen looking at the efficiency and power consumptions in different stages.

## V. Conclusion

A systemic procedure is described to explain the variation of gain with dc voltage bias, device size and matching conditions, considering a simple model to extract the intrinsic parameters. If a more complex model is analyzed, the expression will be more accurate but the procedure for optimization will essentially be the same. The same trend of variation for linearity with device size is observed from IP3 measurements. This confirms the

importance of selection of the device size for enhancing the performance of an RF amplifier.

## REFERENCES


[1] Qingqing Liang et. al.," Geometry and bias current optimization for SiGe HBT cascode low-noise amplifiers", Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE Proceedings of, pp. 407–410, June 2002.

[2] W. Guo, D. Huang, "Noise and linearity optimization methods for a 1.9 GHz low noise amplifier", Third International conference on Microwave and Millimeter-wave Technology proceedings, pp. 923-927, 2002.

[3] Guofu Niu et. al., "Systemic analysis of RF distortions in SiGe HBTs", Radio Frequency Integrated Circuits(RFIC) Symposium, IEEE Proceedings of, pp. 147-150, June 2001.

[4] Guofu Niu et. al., "RF linearity characteristics of SiGe HBTs", Microwave Theory and Techniques, IEEE Transactions on , vol. 49, issue: 9, pp. 1558–1565, Sept. 2001.

[5] N. Srirattana et. al., "A scalable small-signal model for MOSFET including substrate network", Asia specific microwave conference, IEEE Proceedings of, pp. 1203-1206, Nov. 2003.

[6] Sanghoon Kang et. al., "Linearity analysis of CMOS for RF application", Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE Proceedings of, pp. 363 –366, June 2002.

[7] D. M Pozar " Microwave Engineering", John Wiley & sons,1988.


## APPENDIX I: Extracted device parameters

| Width (μm) | $g_m$ (mS) | $g_{ds}$ (mS) | $C_{gs}$ (pF) | $C_{gd}$ (pF) |
|---|---|---|---|---|
| 200 | 42 | 1.17 | 0.25 | 0.05 |
| 400 | 84 | 2.34 | 0.49 | 0.11 |
| 600 | 128 | 3.64 | 0.74 | 0.17 |
| 800 | 170 | 4.9 | 0.99 | 0.23 |
| 1200 | 253 | 7.63 | 1.49 | 0.34 |
| 2400 | 512 | 16.1 | 2.95 | 0.71 |
| 4800 | 974 | 34.5 | 6.20 | 1.45 |