10 Gbit/s Differential Amplifier Demonstrating Striplines in 0.18µm CMOS Technology

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***Abstract* — We demonstrate the differential amplifier using striplines in 0.18µm CMOS technology. A test circuit has single-phase gain of 6 dB and 6.2 GHz bandwidth. Eye diagram of the amplifier at 10Gb/s shows good eye opening. This gives the possibilities for using the strip lines in circuits where over all good shielding is needed.**

I. Introduction

Traditionally, high-speed circuits were realized either in GaAs or in InP technology. Recently, the SiGe technology became an alternative to both. However, these technologies all together have relatively high cost of integration. An approach that will drastically reduce the cost is the standard CMOS technology.

The CMOS technology has a high packaging density and relatively low power dissipation. On the other hand, it is relatively slow. It is indeed difficult to implement passive structures because of high propagation loss due to low bulk-resistivity [1]. In this paper, a single-stage differential pre-amplifier, followed by three pairs of spatially distributed common source stages using striplines, is implemented in standard 0.18µm CMOS technology. Although, striplines (SL's) are lossy as compared to microstrips (MS's) or coplanar lines (CPW's), SL has a certain advantage over both of them, when they are used in complex analogue circuitry for system implementation [2]. In addition, since the dielectric completely surrounds the striplines, they are rather free from dispersion effects.

II. Realization Of Transmission Line Structures

Topside microstrips, coplanar wave-guides and striplines have been simulated by Momentum Electromagnetic Field Simulator and LineCalc (ADS). 50Ω lines are fabricated using standard 0.18µm CMOS process, and modeled from measured S parameter. The characteristic MS impedance is controlled by the width of the conductor ribbon in top metal (M6), which is deposed on the dielectric, with ground metallization in M1 metal to prevent any interaction with lossy substrate. Varying the conductor width from 29µm to 3µm, changes the characteristic impedance in a range of 30-100Ω (Fig.1). Measured attenuation for a 50Ω MS line at 10 GHz is 0.45dB/mm (Fig.2).

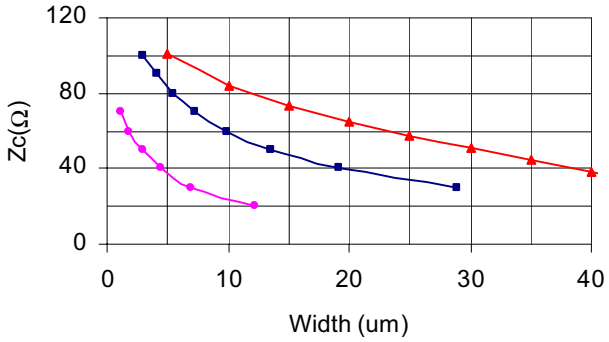

Fig. 1. Characteristic impedance Zc in function of width (MS, CPW for W+G=50, SL)

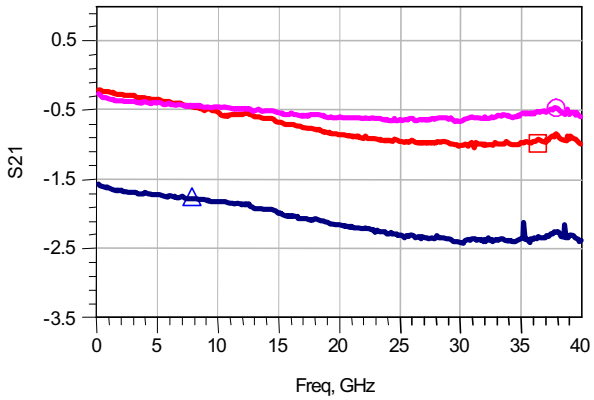

Fig.2. Comparison of measured MS (O), CPW ( ) and SL (Δ) data for the magnitude S_{21}

The CPW uses M6 metallization. The measured attenuation of a 50Ω CPW, obtained for minimum total loss in a frequency range up to 10GHz, is 0.4dB at 10GHz (Fig.2). The characteristic impedance of the CPW is in a range of 40-100Ω while keeping the W+G=50µm (Fig.1).

Stripline is placed in the metal M4, which is in between two parallel metal planes M1and M6. Since the ground planes introduce a large capacitance, striplines are realized with narrow width. As a result, the attenuation of SL is large as compared to MS and CPW, typically 1.75dB/mm at 10 GHz (Fig.2). Changing the conductor width from 12-2µm, changes the characteristic impedance in a range of 20 - 60Ω (Fig.1).

To extract the transmission line parameters, test structures as well as the open structures for pad calibration have been realized on chip. The transmission structures are characterized by S-parameter measurement in the frequency range from 100 MHz to 40 GHz (Fig.2). From the measured S parameter data, the simulation models up to 20 GHz are developed. The transmission structure is treated as a piece of interconnect with propagation constant γ and characteristic impedance Z [3]. An infinite small section of the directly extracted Telegrapher's model of a MS, CPW and SL, with G set to 0, is represented as a two-port network. It incorporates distributed circuit elements R, L, C with their values given per mm length in Table I.

TABLE I:
DISTRIBUTED CIRCUIT PARAMETERS R, L, C

Type of TL	R(Ω/mm)	L(nH/mm)	C(pF/mm)
MS	5.2	0.32	0.13
CPW	5.0	0.28	0.17
SL	22.5	0.30	0.19

Extracted distributed resistance R of SL is almost four times larger then resistance of MS and CPW. Consequently, the attenuation of SL is also much larger compared to the attenuation of MS and CPW.

III. AMPLIFIER DESIGN

To demonstrate co-integration of lumped and distributed amplifier blocks with signal propagation over narrow stripline a differential amplifier that consists of one differential stage followed by three pairs of distributed common source stages is realized.

The input signals are fed into a differential preamplifier circuit (Fig. 3). The two output signals from the differential stage are then used to drive common source stages, which operate from a single 1.8V power supply. Differential inputs are biased at the level of 1.3 V. The input stage features on-chip 50Ω resistors to provide good impedance match. A total length of the stripline's in each branch is 665µm.

Figure 4 shows a microphotograph of the fabricated amplifier. The circuit elements are arranged symmetrically in layout to minimize the offset. Shunt capacitors are connected between the supply voltages and ground. The power dissipation is 185mW on a chip having an active area of 0.5mm^2.

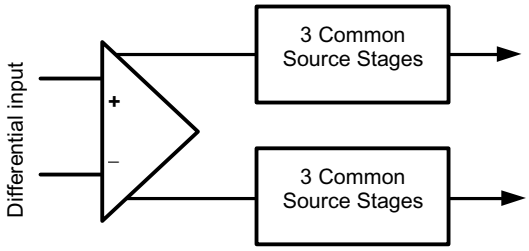

Fig. 3: Block diagram of the differential amplifier

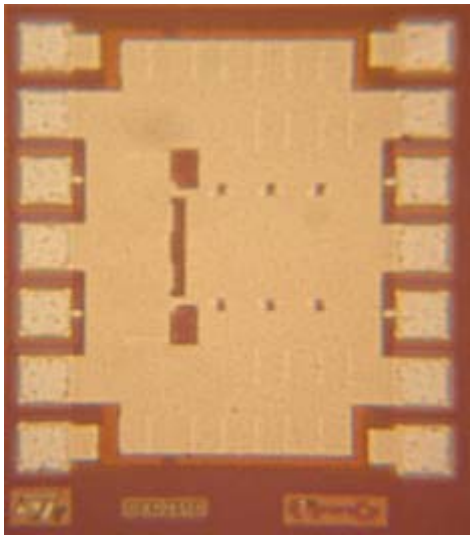

Fig.4. Microphotograph of the realized chip

The simulated S_{21} parameter as a function of frequency is shown in Fig.5. The simulated gain is ~11.5 dB over the 7GHz range. The characteristic frequency response of the amplifier is measured with the wafer probe station and a network analyzer. During this measurement, the other differential input and the corresponding output is terminated with a 50Ω resistor.

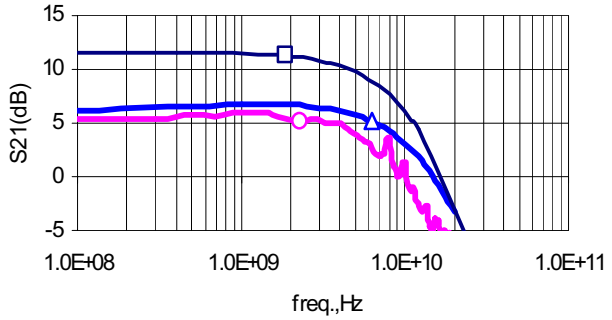

Fig. 5. Comparison of measured (O), simulated (Δ) single phase and simulated ( ) differential magnitude of S_{21}

The measured gain and 3dB bandwidth is ~6dB and 6.2GHz respectively, as shown in Fig.5. To compare simulated and measured results, simulated S_{21} for single-phase input is also displayed. The simulated frequency response includes the effect of striplines but not the effect of parasitic layout capacitances. Thus, there is a slight mismatch of simulated and measured S_{21} parameter. Measured input and output reflection coefficients show

acceptable performance. S_{11} is typically below -9.5dB and S_{22} is below -7dB up to 10GHz range, as shown in Fig.6 and Fig.7. The differential structure also rejects the common mode interferences by 8 to 16 dB over 10GHz frequency range.

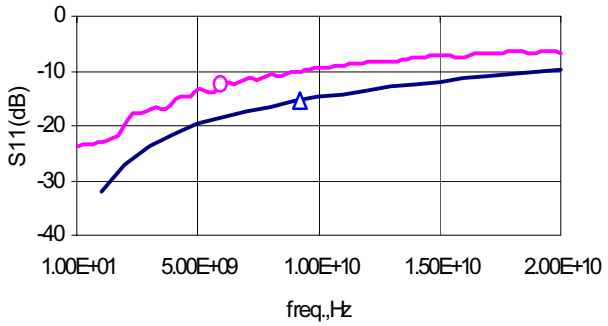

Fig. 6. Comparison of measured (O) and simulated (Δ) single-phase magnitude of S_{11}

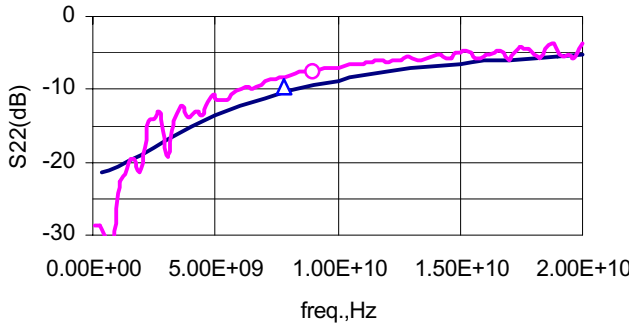

Fig. 7. Comparison of measured (O) and simulated (Δ) single-phase magnitude of S_{22}

The differential amplifier was investigated by eye pattern using single phase 2^7-1 PRBS from pattern generator. Figure 8 shows the exemplary eye pattern recorded at 10 Gb/s for 50mV_{pp} input signal.

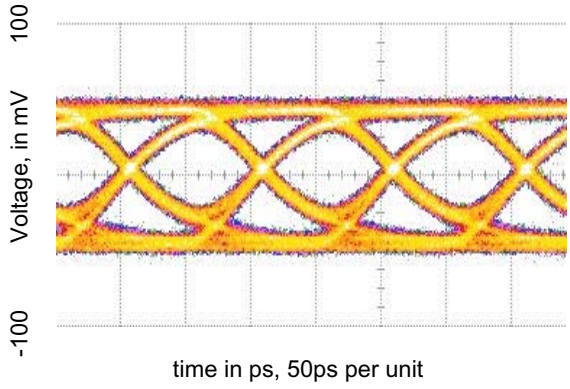

Fig. 8. The measured eye diagram at 10Gb/s for 2^7-1 PRBS input

VI. Conclusion

Simulation models for the MS, CPW and SL are extracted to give fundamental insight on transmission line structures realized in CMOS. A differential amplifier using model data was designed and fabricated. It demonstrates the 10 Gbit/s signal propagation over narrow CMOS strip lines. For a single-phase input, amplifier has the gain of ~6B at 10Gb/s. The measured bandwidth is 6.2GHz.

This CMOS circuit using striplines exhibits still comparable performances with that of the state-of-the-art amplifiers designed in conventional technologies [4], [5]. This opens the possibility for using striplines with its over all good shielding in complex analog systems.

Acknowledgement

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