A Novel Package Approach for Multichip Modules based on Anisotropic Conductive Adhesives

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***Abstract* — In this paper anisotropic conductive pastes (ACP) are proposed for different level interconnections of millimeter-wave multichip modules (MCM) and packages. A novel ACP-based approach for cavity-up millimeter-wave packages simultaneously featuring small size, electrical and mechanical interconnection as well as heat transfer capabilities is presented.**

I. Introduction

MULTICHIP modules using flipchip technology as 1st level interconnect are becoming more and more popular to address the ever increasing demand for higher packaging densities at higher frequencies.

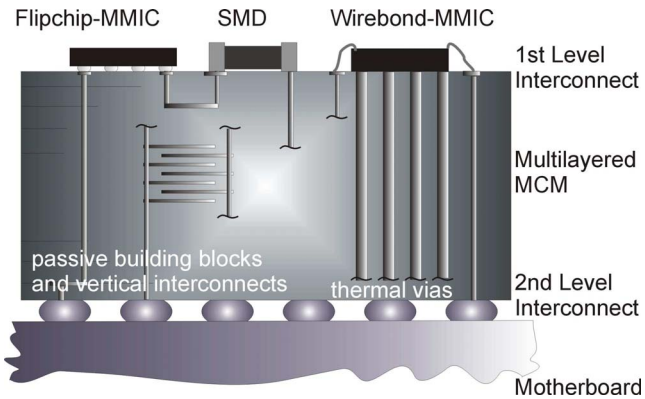

Fig. 1. Typical module concept.

Fig. 1 depicts a module concept based on multilayered substrate technologies such as low temperature co-fired ceramics (LTCC). In case of multilayered modules the signal and control lines are vertically routed from the 1st level interconnects to the bottom side of the module. The 2nd level interconnect, i.e. the interconnection between the module and its motherboard, is established by standard surface mount technologies like ball grid arrays. Multiple passive functions can be integrated in the inner layers of the multilayer MCM [1, 2].

Following this approach low cost thermal management solutions are usually based on thermal vias transferring heat from dissipated power from active components all through the module to a heat sink on the bottom side. Unfavorable to the passive integration task, the space required by these thermal vias within the module can no longer be allocated to passive building blocks like filters and couplers.

Here, a novel approach for cavity-up millimeter-wave packages simultaneously featuring small size, electrical and mechanical interconnection as well as thermal management capabilities is proposed.

Recent results on ACP-based 1st level flipchip interconnections up to 110 GHz [3] and 2nd level interconnections [1] motivate to utilize ACP also for other millimeter-wave interconnections and package approaches.

These results are briefly sketched demonstrating the potential of ACP-based interconnections. Then, complementary to [1] and [3], the application of ACP to novel millimeter-wave package solutions is presented

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II. ACP-Flipchip Interconnection

In a typical flipchip configuration bumps provide electrical and mechanical connection of the chip mounted upside down on the substrate. Usually these bumps are fabricated by a modified ball bond process (studbumps) or by gold plating [4] on either the substrate or the chip.

Flipchip technology meets fine-pitch requirements for millimeter-wave integrated circuits (MMIC) and has already been proven to be a promising alternative to wirebond interconnections up to W-band frequencies [5, 6]. Instead of studbumps conductive adhesives can be applied as well for bump fabrication up to these frequencies. Additional usage of photoresist allows bump formation and provides chip support [7].

Anisotropic conductive adhesives are usually applied

to interconnect flexible displays [8]. They are composed of adhesive polymers filled with conductive particles as small as 4µm to 5µm. When applied between two surfaces and thermocompression bonded a permanent joint is realized. In areas where the particles are squeezed conductivity is provided.

In [3] anisotropic conductive paste is applied to millimeter-wave flipchip interconnections in a novel approach. It follows from the modified dispense technique applied to isotropic conductive adhesives in [7]. In combination with structured dielectric layers ACP builds the 1st level interconnect compatible with fine-pitch flipchip technology. Experimental results validated the functionality of ACP up to millimeter-wave frequencies. The transmission loss per single ACP flipchip transition remained below 0.5dB (0.75dB) up to 100GHz (110GHz).

In [1] it has already been demonstrated that standard 2nd level interconnections (e.g. ball grid array in Fig. 1) can also be replaced by ACP in millimeter-wave LTCC packages.

III. Novel Cavity-up ACP Package

These results on 1st and 2nd level interconnections demonstrate the potential of ACP as alternative to conventional interconnection technologies. As will be discussed next, ACP can advantageously be applied to MCM leading to novel millimeter-wave packaging solutions.

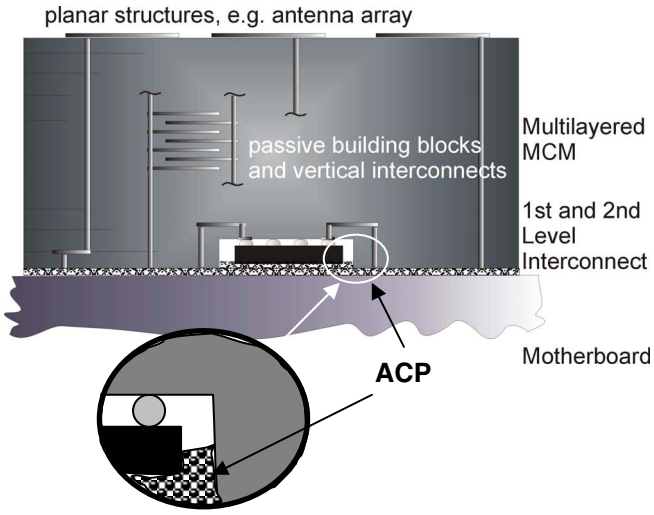

Fig. 2 Millimeter-wave cavity-up ACP package and detailed view of MMIC in cavity.

Fig. 2 illustrates how ACP can be used in combination with cavities featuring multiple functions in addition to rf- and dc-signal routing. The active components (e.g. MMIC) are flipchip-mounted in cavities on the bottom side of the multilayered module (e.g. LTCC).

The module is attached to a motherboard utilizing ACP. The ACP provides mechanical, thermal and electrical interconnection between the module and the motherboard. In order to avoid contamination of the 1st level interconnect the cavity is not completely filled with ACP (see enlarged view for details). By this approach, the chip is encapsulated and beneficially its rf-performance is not degraded by the encapsulating material.

Furthermore, heat transfer capabilities are established via the backside of the chip. Thermal vias can exclusively be implemented in the motherboard. Since thermal vias are not required inside the multilayered module more space is available for passive building blocks and rf- and dc-signal lines. In contrast to Fig. 1 the rf- and dc-signals from the MMIC do not have to be routed all through the module. The top side of the module can be used for other passives like planar antennas.

Next, the electrical and thermal performance of this package concept is analytically and experimentally investigated.

A. *Electrical Performance*

Fig. 3 depicts an exploded view of a suitable test structure and Fig. 4 shows the realized corresponding test package before final assembly. In a first step, Rogers' RO4003 and TMM-substrate are chosen as substrate material. R04003 is used as motherboard.

Two stacked TMM-substrates build the multilayered module. The upper TMM-substrate carries two interrupted 50Ω CPW lines that are bridged by a flipchip test device (50Ω CPW line with fine-pitch dimensions). The second TMM substrate provides the vias for vertically rf-routing (minimum via diameter and pitch are 0.3mm and 0.7mm, respectively). Furthermore it has a cavity for the test device in its center (cavity dimensions are 5mm x 2mm x 0.38mm). Both TMM substrates have two more cavities at their edges to allow on-wafer probes to be connected to the CPW lines on the R04003 after final assembly. After flipchip-mounting the test device, the two TMM substrates are stacked (1). The overall thickness of the assembled TMM-module is 760µm. This module is attached to the R04003 motherboard (2) utilizing ACP.

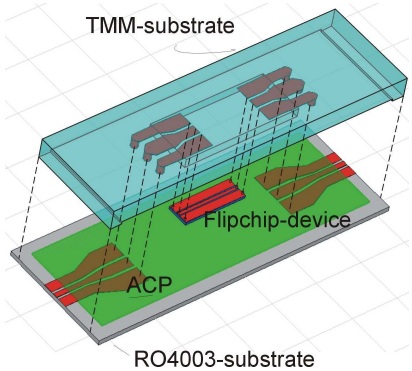

Fig. 3. Exploded view of a test structure.

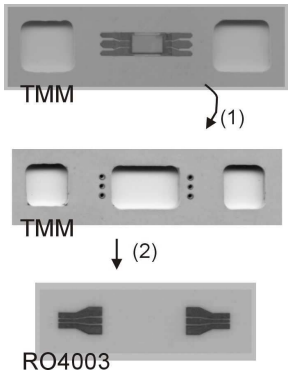

Fig. 4. Test package before final assembly.

Fig. 5 shows the simulated electrical performance of a test package with a flipchip test device inside the cavity. For comparison results for a test package with a plain CPW on the upper TMM substrate instead of a flipchip test device are shown as well.

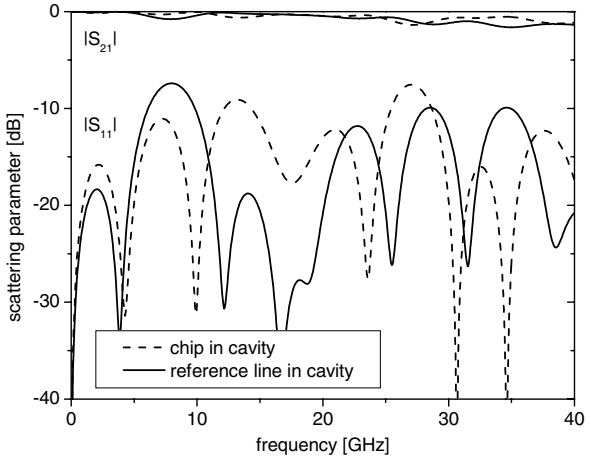

Fig. 5 Simulated scattering parameters of cavity-up package according to Fig. 3 and Fig. 4.

In both cases the input reflection of this back-to-back arrangement remains below –7.5dB between 0 and 40GHz while the transmission is better than –1.6dB. Within the boundaries set by the manual manufacturing process a further optimization of these test structures is not possible.

The scattering parameter measurements of the corresponding assembled test structures are depicted in Fig. 6. The input reflection of the test package with and without flipchipped device are on the same order as the predicted values up to 30GHz. The transmission of the test package with flipchipped device in the cavity is comparable to the reference structure without flipchipped test device up to 22GHz. The higher transmission loss compared to the simulations can be related to the above mentioned manufacturing limitations with respect to manually assembly, via drilling and filling.

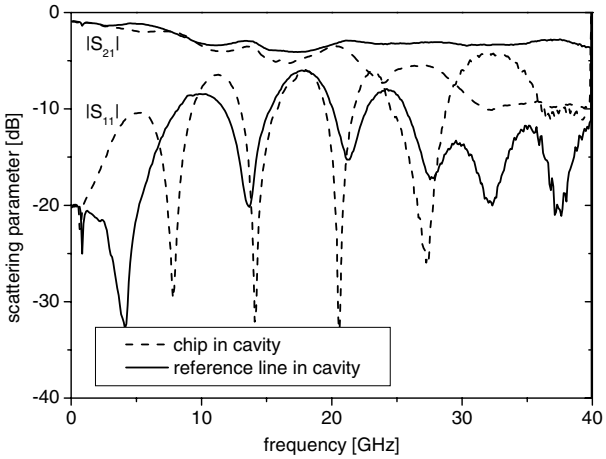

Fig. 6 Measured scattering parameters of cavity-up package according to Fig. 4.

Taking these uncertainties into account, these first test structures already demonstrate the feasibility of the approach. Results on 1st level interconnects in Section II and on 2nd level interconnects in [1] using ACP promise even better performance up to higher frequencies.

B. Thermal Management

Beside the encapsulation and rf- as well as dc-interconnectivity in combination with low parasitics on the rf-signal, the cavity-up ACP package offers simultaneously thermal management without impairing the passive integration capabilities. Fig. 7 depicts a measurement setup suitable to experimentally validate its thermal performance. Now, instead of the flipchip test device a SMD resistor is mounted in the cavity of the TMM substrate.

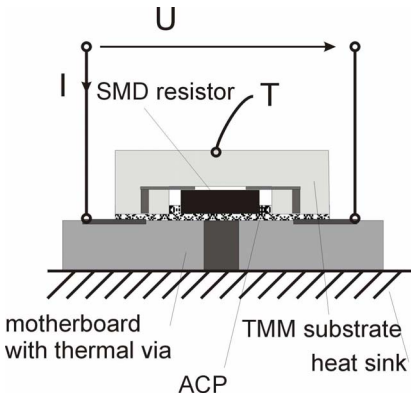

Fig. 7. Thermal management measurement setup.

A dc-signal is supplied to the resistor. The applied voltage U, current consumption I, and temperature T are monitored. Fig. 8 plots the temperature T close to the cavity versus the dissipated power for different measurement setups.

The first configuration is the TMM-package with SMD resistor not connected to the motherboard. Then, this

module is mounted on the motherboard. Finally, the setup as depicted in Fig. 7, consisting of the SMD-type resistor in cavity, on motherboard with thermal via and heat sink is investigated. It can be seen that the heat generated by the device is well transferred to the heat sink. At 1 watt of power per 1.28mm^2 chip area the temperature within the package remains below 80 degree celcius, i.e. within specifications of standard amplifier MMIC.

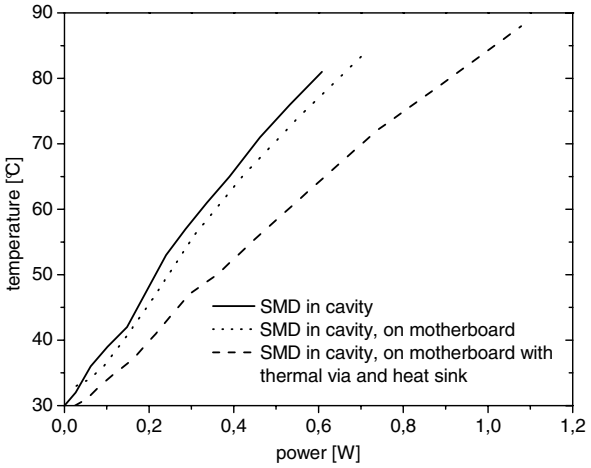

Fig. 8. Experimental study of thermal management capability.

IV. Conclusion

This paper reports on ACP-based millimeter-wave interconnections. The anisotropic conductive characteristic of the adhesive reduces the assembly efforts and the complexity of the joints. A novel millimeter-wave ACP package solution is proposed. MMIC can be mounted in cavities on the bottom side of the MCM in a flipchip approach. ACP provides encapsulation, electrical and mechanical interconnection to a motherboard as well as thermal management capabilities.

References

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