HIGH TEMPERATURE PERFORMANCE OF GAN-BASED HFET'S

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ABSTRACT

The technological building blocks for high temperature HFET devices are described. The RF characteristics are investigated by on-wafer testing up to 200°C and the DC characteristics are evaluated up to 850°C in vacuum. Permanent degradation is observed above 650°C. It is concluded, that the chemical stability of the heterostructure material itself may be mainly responsible for this limit.

INTRODUCTION

GaN is a wide bandgap material with high breakdown strength and high figures of merit for power operation and may thus be attractive for both high temperature and high power, high speed operation [1]. Microwave power densities in the order of 10 to 20 W/mm are predicted for GaN-based heterostructure FET's [2]. The maximum power density experimentally extracted is steadily improving, presently reaching 6.9 W/mm [3]. Operating at these power densities means operation at elevated temperature (>250°C) even for substrates with high thermal conductivity like SiC. Since GaN is a wide bandgap material (E_g>3eV), even at 1000°C the intrinsic carrier concentration for the ideal crystal is below $10^{12}cm^{-3}$ and the bandgap energy will not dominate the high temperature/high power device performance. Thus, GaN based FET structures offer the potential of high speed, high power and high temperature operation beyond that of Si and GaAs.

However, SOI-MOS and GaAs based HFET device structures have been operated successfully up to 400°C and 500°C respectively under quasi-static conditions [4,5] and GaN device operation needs to surpass these temperatures essentially to demonstrate an essential improvement.
In general, continuous degradation of RF gain, noise and power may be observed already at moderate temperatures due to the temperature dependence of the electronic properties like carrier mobility and overshoot velocity [6]. At high temperature the thermal limit of the chemical materials and interface stabilities may be reached, seriously degrading reliability [7]. This concerns the contacts, the surface and the heterostructure material itself and has lead to high temperature stable metallization and passivation schemes in the case of conventional III-V semiconductors, which have also served as initial basis for the development of a high temperature stable GaN device technology.

HIGH TEMPERATURE CONTACTS

Current GaN-based FET devices contain an AlGaN/GaN heterostructure with GaN-channel, the channel sheet charge being generated by direct doping, modulation doping from the AlGaN barrier or by piezo-induced charge. Thus, ohmic contacts need to be made to this GaN-channel and Schottky control contacts to the AlGaN layer.

GaN is a semiconductor of high ionicity and the electron affinity dominated by the Ga work function [8]. Thus, GaN belongs to the materials with a direct dependence of the Schottky barrier height on the metal-semiconductor work function difference [9] and metals with a low work function (Al, Ti) are used for ohmic contacts to n-GaN and metals with high work function are used for Schottky barrier contacts (Pt, Ni, Au, Ir, Pd). There are still large variations in barrier height reported by different workers for standard metals on GaN. This indicates that surface preparation still has a major influence. The nitride forming elements may create near surface nitrogen vacancies and an n^+-doped junction.
Adding Al to the compound weakens the dependence of barrier height on the metal work functionas is observed for Au. The barrier height itself increases [10].

The overlay metallization is commonly Au and therefore a diffusion barrier is needed for high temperature operation. In reference to the standard high temperature GaAs device technology an amorphous W:Si:N compound may be employed [11]. This metallization scheme represents a high thermal stability and suppresses Au-diffusion up to temperatures above 1000°C. The stability is improved with increasing N-content, which prevents re-crystallization and stuffs residual grain boundaries. However, the conductivity of the alloy is highly reduced with high N-content and a compromise needs to be found in respect to the contact resistance.

Ti and Al in multilayer stacks or as alloy are commonly used in todays ohmic contact technology of FET's. A peritectic $TiAl_3$-alloy needs to be formed. For higher Al-content liquid Al may remain above the peritectic liquidus line above 660°C, seriously limiting the high temperature stability. The contacts are formed on the AlGaN barrier layer or in dry etched trenches. They are generally annealed at 600°C to 900°C by RTA. A contact resistance down to 10^{-7} Ωcm^2 has been reported on n-GaN [12]; on AlGaN the contacts may become progressively non-linear due to a residual barrier for an Al-content above 10%. For high thermal stability Ti and W have been investigated in combination with W:Si and W:Si:N barriers [13,14]. Fig.1a shows a Ti/W:Si:N/Au contact deposited into a sputter-etched trench onto the n-GaN channel and alloyed at 860°C by RTA for 20 sec.. Fig.1b shows the electrical characteristics under operation up to 850°C. No degradation in electrical performance nor morphology was observed after this test. The W:Si:N diffusion barrier was sputter deposited under high nitrogen partial pressure and the barrier very effective in blocking the diffusion of Au. However, the electrical conductivity across this barrier was also highly reduced resulting in an overall contact resistance of 10^{-3} Ωcm^2.

A variety of Schottky metals have been investigated experimentally on n-GaN and n-AlGaN in respect to their forward and reverse IV-characteristics to identify highly rectifying behavior and high reverse breakdown characteristics [15]. The analysis of these IV-characteristics suggests that the interface may be heterogeneous in many cases with small areas of low barrier height, which are surrounded by an area of high doping concentration, and which are in parallel to the large area contact [16]. The physical/chemical origin of the inhomogeneities is not well identified presently and the problem approached by developing specific pre-deposition procedures. In general low barrier defect clusters, which are surrounded by an area of high doping concentration will create field and temperature activated leakage.
In the GaN-HFET technology mostly investigated are Pt, Pd, Ni and recently Ir [17,18] with a barrier height between 0.8 eV and 1.1 eV. It may be worth noting that no chemically stable nitride compound is expected for Pt, Pd and Ir below the melting point of these metals. Only few investigations have considered operation and annealing at high temperature. Detailed studies on the interfacial conditions and reactions are still outstanding. For Pd interfacial reactions are infered due to changes in barrier height after annealing at around 400°C [17]. For Pt, thermal stability has been reported for annealing at 400°C for 1 hr [18]. For Ni, nitride formation is seen already above 200°C and complex reactions also with Ga above 400°C [19]. Initial experiments with Ir show stable reverse characteristics after annealing at 400°C for 120 hrs [20].

In this investigation Pt/Au Schottky contacts have been used. Fig.2a and fig.2b show IV-characteristics for 2 thermal cycling experiments: In Fig.2a the forward and reverse characteristics are plotted for R. T. and 600°C. A strong thermal activation of the reverse leakage current is observed, which can be explained by the above mentioned thermal activation of defects [9]. If evenly distributed their density may be estimated to $10^{-8}cm^{-2}$. Also seen is an increase of forward current level due to the activation of deep donors in the AlGaN layer. Cooling the diode back to R. T., the forward characteristic is totally recovered and the reverse characteristic improved, indicating the passivation or elimination of part of the defects. In a second experiment the cycling temperature was increased to 750°C. Again, a strong thermal activation of the reverse current is observed. Upon cooling the initial R. T. characteristic is again slightly improved, again indicating a reduction in active defect sites. But now also the forward characteristic is changed and the barrier height decreased to 0.45eV. This seems a degradation, but such a degradation is not reflected neither in the reverse current levels nor in the breakdown behavior. In fact at 750°C the on/off ratio is still nearly one order of magnitude and large enough to pinch off the FET device as is shown below. The above results show that indeed the characteristics are entirely dominated by the behavior of defects and not related to the barrier of the large area contact. The change in barrier height during annealing between 600°C and 750°C may allow the speculation that in this temperature range Ga-oxide is reduced and the interfacial Ga absorbed by the Pt, forming a stable Pt:Ga/AlGaN interface.

HETEROSTRUCTURE MATERIAL AND SURFACE

The buffer layer is one of the critical elements in the high temperature FET performance, because it needs to maintain its semi-insulating characteristics. In the past, GaN-buffer layers have displayed high thermal activation in their conductivity due to a high defect density, and high temperature operation of FET's has been limited to approx. 500°C by this effect [21, 22]. Recent advances in buffer layer growth have resulted in essentially stable semi-insulating characteristics up to 400°C with an activation energy as low as 20 meV. However, above 400°C high thermal activation is still seen. This high temperature branch in the buffer layer conduction can be associated either with conduction in the buffer layer or the surface. Therefore, a temperature cycling experiment was performed in different ambients. Fig. 3 shows the conductance between two mesas after dry etching and after termination of the entire device processing sequence including lithography, contact deposition, patterning and ohmic contact alloying, followed by thermal degazing in vacuum at 500°C. The behavior is reversible. Also shown is the same device area after strong oxidation in oxygen atmosphere at 500°C. Up to 400°C an identical conductivity to that of the first experiment is observed. However, between 400°C and 450°C a steep rise by

nearly 3 orders in magnetude is encountered. Subsequent cycles follow the behavior as initially. Thus, it may be concluded that the steep rise in conductivity is connected to a re-arrangement of the surface condition, probably desorption of adsorbates, which were deposited or generated by the high temperature oxidation step.
Despite the high activation of the conductivity at high temperature, FET operation was possible up to 750°C as shown below.

It seems that the electronic state of the GaN surface (and also that of AlGaN) and surface conductivity may play an important role in FET devices. This seems not surprising, since semi-insulating GaN (and also AlGaN) is a highly polar dielectric and the adsorption of poplar molecules on the surface seems reasonable. However, the correlation with surface conductivity is not clear yet. This points towards GaN device passivation. This subject however has not yet been discussed seriously.

The FET channel characteristics have been investigated by temperature dependent Hall measurements up to 600°C. In this investigation a doped channel FET structure was investigated with an initial R. T. mobility of 230 cm^2/Vs. Up to 150°C the mobility value droped slowly, above 200°C the decrease followed a $T^{-3/2}$ power law as expected for phonon dominated scattering. The temperature limit was determined by resolution limit for the Hall signal. At 600°C a mobility of $100cm^2/Vs$ was extracted [23].

FET DEVICE CHARACTERISTICS

The devices have been tested in two ways. DC thermal stress experiments were carried out up to 850°C in vacuum and microwave testing was performed on-wafer up to 200°C limited by the thermal stability of the probes used.

The first experiment was performed as follows: In vacuum the samples have been heated in intervalls of 50°C holding them at each temperature for 20 min. During this time the device was continuously tested by on-wafer bias scans. In between each temperature step the sample was cooled down and R. T. data were taken to distinguish between reversible phenomena and permanent degradation. Such an experiment up to 600°C is shown in fig. 4. It is seen, that no major degradation has occured during the temperature cycling experiment and the open channel saturation current is fully recovered after cooling. In fact, during the temperature stress the ohmic contacts have been improved decreasing the on-resistance. Above 600°C the changes were irreversible. Fig.5 a, b show the output characteristics of the identical device at 750°C and after cooling down. After cooling the current does not recover. After cooling from 800°C, an open channel current of only 0.2 mA/mm is detected at a reduced pinch-off voltage of –2V; and an ungated FET channel showed a saturation current of 0.4 mA/mm (see fig. 6). After 850°C temperature stress the saturated current was reduced by essentially 2 orders of magnitude.
In general we have observed that devices fail as early as at 650°C not related to contact failure. The channel sheet charge N_s and open channel current degrades rapidly and cannot be recovered upon cooling. This has been observed for AlGaN/GaN heterostructures grown by MOCVD as well as grown by MBE and was therefore thought to be a phenomenon related to the heterostructure materials stability. This is illustrated with table 1, where the critical temperature for reduction of the open channel current to 10% of its initial R.T. value is listed for a number of materials and device configurations. Thus, this phenomenon seems indeed correlated with the thermal stability of the heterostruture materials system in the present state of quality
This may become clearer considering the materials thermal/mechanical properties. For GaN the Debye temperature is approx. 750°C and decomposition can be expected above 650°C [24]. Thus, it seems indeed that the mechanical/chemical stability of the material determines its maximum temperature of operation. In this respect it is essentially inferior to its two other wide bandgap materials competitors SiC and diamond with a Debye temperature of 1030°C and 1850°C respectively.

As has become clear, no major degradation may be expected in the small signal microwave performance depending on the design of the structure. Indeed, testing a 1µm gatelength device with a doped channel resulted in nearly unchanged cut-off frequencies f_T and f_{max} between R. T. and 200°C (figs. 7a,b).
The large signal and power performance shows a more complex behavior, because in many device structures another effect is entering. This is the compression in microwave power in comparison to quasi-DC. This effect has been traced back to a compression in current, which can be modulated by RF, above a characteritistic transition frequency [24]. This effect does also show a thermal activation and thus the transition frequency is temperature dependent, shifting to higher values at higher temperatures. Imagine the following experiment: a device is operated above the transition frequency in the upper MHz-range at a certain bias point and load line. The RF power is essentially lower than expected from the DC characteristics. Turning up the drain bias further using the same load line should result in a reduction in output power due to increased self heating and reduction in channel mobility. However the self heating might also shift the transition frequency across the frequency of

operation and the output power may increase instead. Thus, the RF-power may increase with increasing temperature. Such a case in illustrated in fig. 8a,b. However, it should be realized that this increase is only due to a parasitic effect in the first place.

CONCLUSION

During recent years the technology of GaN-based heterostructure FET devices for high speed, high power/high temperature applications has been intensively persued and power densities approach now half the values of what may be expected ultimately. This high power handling capability, which stems mainly from the high materials breakdown field, poses high demands on the thermal management and the reliability during operation under high internal temperature stress. It seems that the chemical heterostructure material stability will ultimately limit the maximum operating temperature, although the role of defects is not clear and activation energies for this degradation phenomenen have not been determined yet. Thus, the area of save operation has not been determined yet, but may be as high as 600°C. Questions concerning the materials quality and surface passivation are also still open.

The thermal management seems demanding, but thermal simulations [1] indicate that using SiC and diamond heat spreaders will allow to utilize the potential to such an extent that the bottle neck may be shifted towards the packaging and heatsinking part. The development of high power/high temperature packaging seems therefore the most urgent requirement at present.

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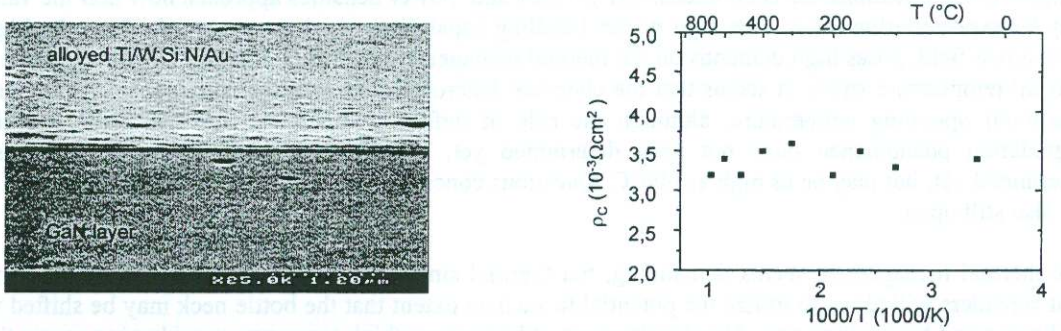

Fig.1a,b:
Micrograph (a) and specific contact resistance (b) from TLM measurements of a Ti/W:Si:N/Au contact to n-GaN as function of operating temperature. The contact was successively heated in vacuum in steps as indicated and held 20 min at each temperature.

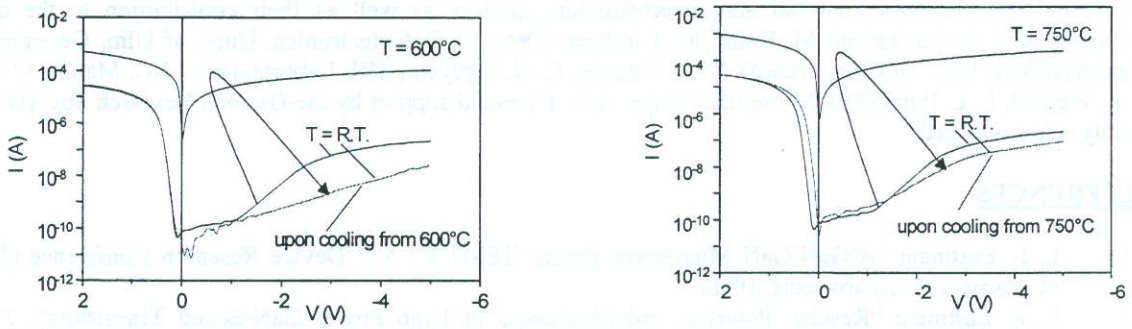

Fig.2 a,b:
Thermal cycling of Pt-AlGaN Schottky diodes with 10% Al. IV-characteristics are shown before temperature stress, during and after. In fig.2a the stress temperature was 600°C, in fig.2b this was 750°C in vacuum.

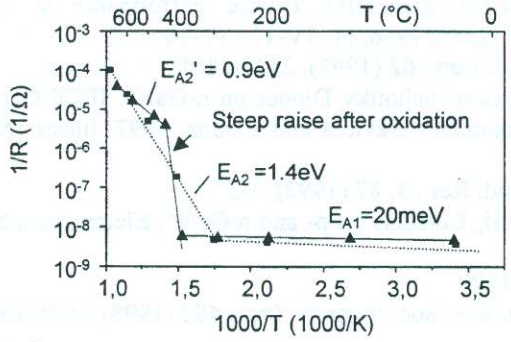

Fig. 3:
Temperature dependant conduction between 2 100µm wide mesas with 5µm separation of GaN FET MOCVD buffer layer on sapphire.
Solid line: initial stress experiment as indicated in text.
Dashed line: stress experiment after oxidation.

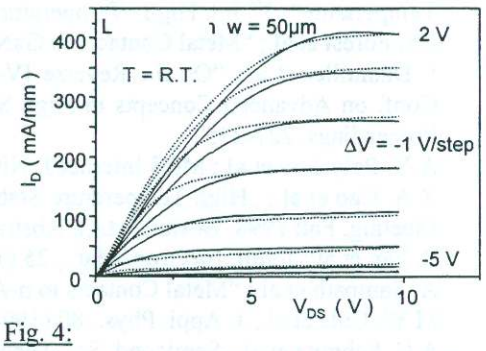

Fig. 4:
IV-characteristics of doped channel HFET at R.T. (solid line) and after stressing (dashed line) up to 600°C as described in the text.

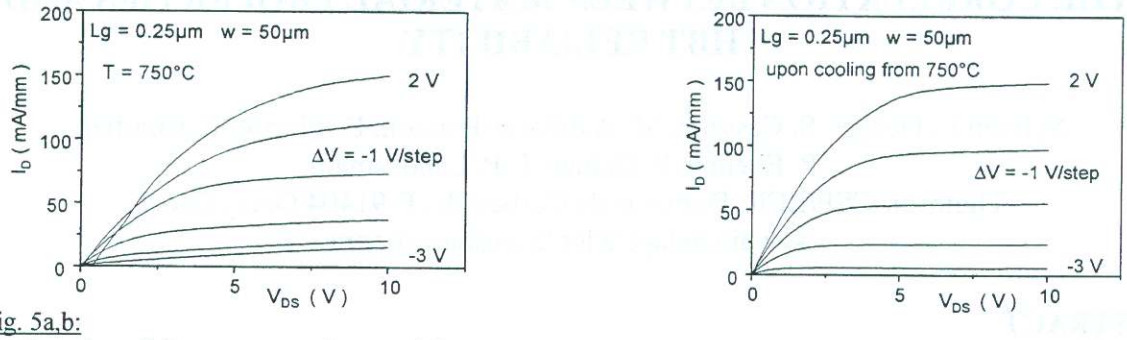

Fig. 5a,b:
Continuation of the stress experiment of fig. 4 up to 750°C and characteristics at this operating temperature (a) and after cooling down to R. T. (b).

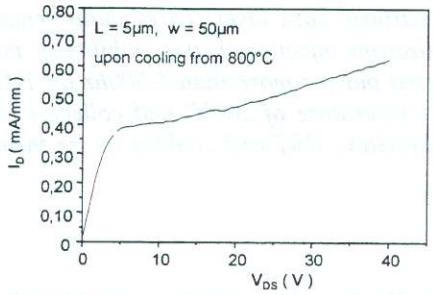

Fig. 6:
Characteristics of an ungated channel after cooling down from 800°C.

SAMPLE	HETEROSTRUCTURE	T (I/I_0 = 0.1)
MBE	AlGaN/GaN (Al=25%) MODFET	650°C
MOCVD(a)	AlGaN/GaN (Al=15%) MODFET	650°C
MOCVD(b)	AlN/GaN (Al=100%) channel doped HFET	650°C
MBE	AlGaN/GaN (Al=26%) MODFET	700°C
MBE	AlGaN/GaN (Al=33%) MODFET	700°C
MOCVD(a)	AlGaN/GaN (Al=18%) channel doped HFET	700°C
MOCVD(b)	AlGaN/GaN (Al=15%) channel doped HFET	750°C
MOCVD(a)	AlGaN/GaN (Al=18%) channel doped HFET	800°C

Table 1:
Summery of HFET stability test as described in the text.

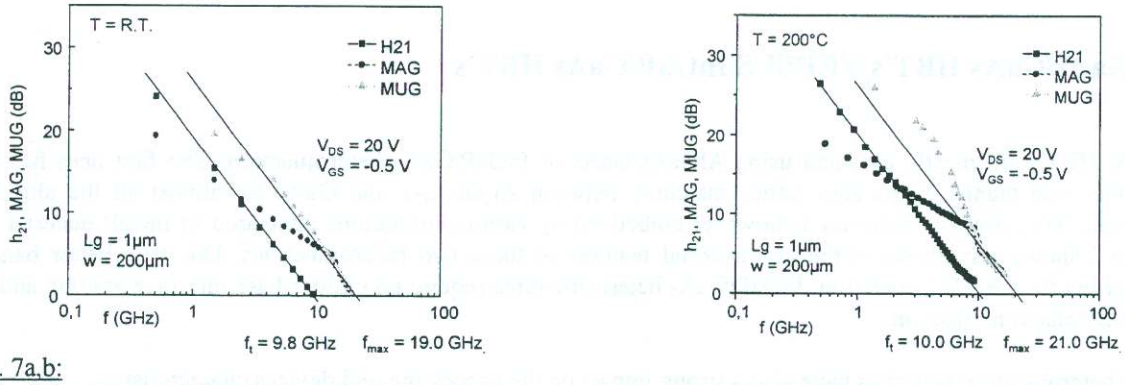

Fig. 7a,b:
Cuf-off frequency of doped-channel AlGaN/GaN HFET with 1 µm gatelength at R. T. (a) and 200°C (b) in the identical bias point.

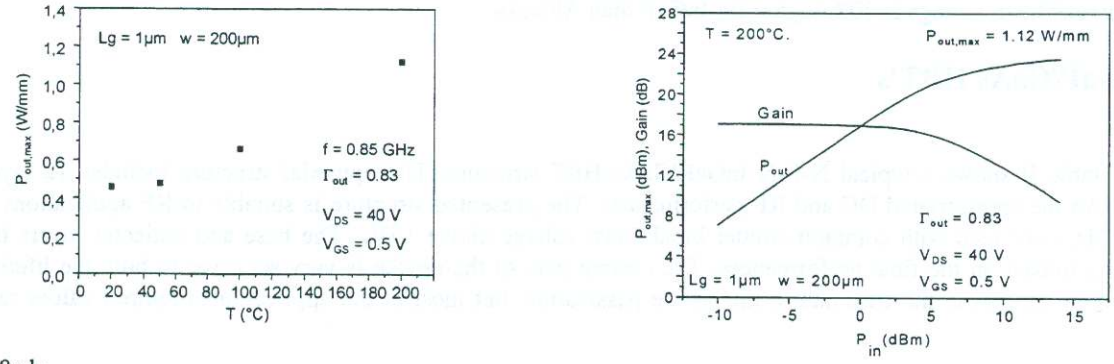

Fig. 8a,b:
(a) Saturated RF-power at 850 MHz as function of temperature. (b) Power and gain curve at 200°C