10-40GHz design in SiGe-BiCMOS and Si-CMOS – linking technology and circuits to maximize performance

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***Abstract* — This paper reviews the relevance of the widely used device metrics f_T, f_{max} as well as the recently introduced device metrics f_A and f_{cross} for broadband circuit design. Usually, IC processes are benchmarked on the basis of their f_T and f_{max}. For most circuit applications however, there is only an indirect relation between f_T, f_{max} and circuit bandwidths. Since the differential pair amplifier is a key building block in broadband circuits, the metric f_A provides a nearly direct relation to broadband circuit performance. This is demonstrated via the maximum operating frequency of a current-mode logic frequency divider, processed in 3 generations of a BiCMOS process. Metric f_{cross} is valuable for the design of circuits employing a cross-coupled differential pair as active negative resistance, such as in LC-VCOs. The metrics can be expressed in terms of transistor parameters (e.g., R_b, C_{bc}, …), allowing to derive a link between circuit performance and technology. Based on our experience, we evaluate IC processes on the basis of f_T, f_A and f_{cross} rather than f_T and f_{max}.**

I. Introduction

It is common practice to use the transition frequency f_T and maximum oscillation frequency f_{max} for benchmarking and IC process optimization. However, since there is only an indirect relation between the device metrics f_T, f_{max} and broadband circuit performance, optimizing a process on the basis of these metrics does not automatically lead to optimum circuit bandwidths. Thus, there is a need for device metrics that provide on the one hand a direct relation to broadband circuit bandwidths and, on the other hand, provide a direct relation to device parameters (i.e., R_b, C_{bc}, …). In this paper, the relevance of two recently introduced device metrics for broadband circuit design is analyzed, namely the available bandwidth f_A [1] and the maximum frequency for which a cross-coupled differential pair provides a negative shunt input resistance f_{cross} [2].

In Section II, the device metric definitions are reviewed for bipolar transistors, and their relation to transistor parameters of a simplified transistor model is provided. In Section III, the evolution of these metrics across 3 generations of a BiCMOS process is reviewed. While the transition from [3] to [4] was driven by metrics f_T and f_{max}, the transition from [4] to [5] was driven by f_T, f_A and f_{cross}. Despite the increase in f_T and f_{max} from [3] to [4], a relatively poor improvement in broadband circuit bandwidths was found. Reversely, the transition from [4] to [5] resulted in a significant circuit performance increase. In Section IV, some circuit examples and their relation to device metrics will be described. Section V highlights the major differences between bipolar and CMOS for f_A and f_{cross}, as well as the implications for broadband circuit design. The paper ends with conclusions in Section VI.

II. Device metrics for bipolar

Although device metrics can be derived directly from measured y-parameters [1], in this paper all metrics are obtained from Spectre circuit simulations. To obtain simple relations between the metrics and transistor parameters, they are evaluated for the simplified equivalent transistor circuit shown in Fig. 1. In all circuits in this section, dc biasing has been omitted.

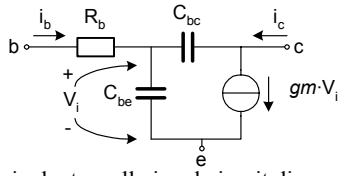

Fig. 1: Equivalent small-signal circuit diagram.

A. f_T and f_{max}

For the derivation of f_T, the base is driven by a current source while the collector is grounded. For the derivation of f_{max}, the base is driven by a port with source impedance Z_s and terminated by a load resistance Z_L, each optimized for power matching. The corresponding circuits are shown in Fig. 2.

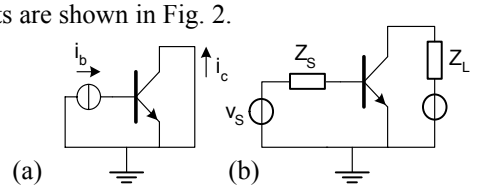

Fig. 2: Schematic to extract f_T (a) and f_{max} (b).

Both configurations are not representative for broadband circuits. The base terminal is usually driven via a low-ohmic source impedance. Metric f_T represents the bandwidth of the current gain of a common-base amplifier. Metric f_{max} has no direct relation to broadband circuit performance, since wideband operation is typically obtained by matching to the interconnect characteristic impedance, and transistor in- and output impedance are considered as parasitics.

A further drawback of metrics f_T and f_{max} is that the peak-values of modern bipolar and CMOS processes are well beyond the measurement capabilities of even the most advanced equipment. Thus, the results rely on extrapolation. Besides, metric f_{max} can be based either on the maximum stable gain or the unilateral gain, which complicates the relation to broadband circuit bandwidths.

B. f_A, f_V and f_{out}

The available bandwidth f_A represents the 3-dB bandwidth of a differential pair amplifier driven by a voltage source, designed for 20 dB low-frequency voltage gain. Across a bias sweep, the load resistance value R_L is adjusted to fix the low-frequency voltage gain to 20 dB. Metric f_A can be sub-divided in two contributions, namely the input bandwidth f_V (representing the bandwidth of the transconductance i_c/v_{be}) and output bandwidth f_{out}. The single-ended equivalent circuits for the derivation of f_V, f_{out} and f_A are shown in Fig. 3.

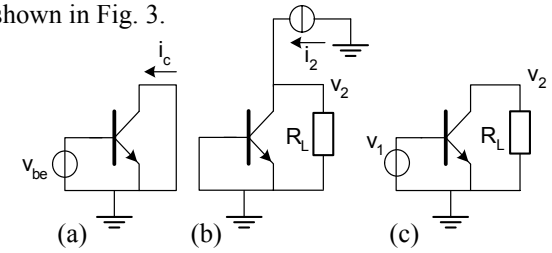

Fig. 3: Schematic to extract f_V (a), f_{out} (b) and f_A (c).

For the equivalent transistor circuit shown in Fig. 1, the following approximations can be derived:

$$f_V = \frac{1}{2\pi R_b (C_{be} + C_{bc})} = \frac{f_T}{gm \cdot R_b} \qquad (1)$$

$$f_{out} = \frac{1}{2\pi R_L C_{bc} (1 + gm \cdot R_b)} = \frac{1}{2\pi R_L C_{22}} \qquad (2)$$

$$f_A = \frac{f_V f_{out}}{f_V + f_{out}} \qquad (3)$$

Here, $C_{22} = C_{bc}(1+gm \cdot R_b)$ is the transistor output capacitance. When evaluating f_A across a bias sweep, the following observations can be made. In the first place, metric f_A is dominated by f_{out} for low currents (where high load resistance values are required due to the low transconductance gm) and by f_V for high currents (where the base-emitter capacitance C_{be} is high). The output capacitance C_{22} is constant at low bias currents, but is proportional to the bias current when $gm \cdot R_b > 1$. This effect is demonstrated in Fig. 4. As a consequence, the output bandwidth saturates for $I_c > V_T/R_b$, with $V_T \approx 25$ mV the thermal voltage. Since the input bandwidth f_V decreases with increasing bias current, the peak-f_A typically occurs at a bias current where $gm \cdot R_b \approx 1$ to 2.

C. f_{cross}

Metric f_{cross} represents the highest frequency for which a cross-coupled differential pair provides a negative shunt input resistance. At f_{cross}, the real part of the input admittance crosses zero. The equivalent circuit for the derivation of f_{cross} is shown in Fig. 5. A virtual ground exists at the common emitter node, where a dc bias current is applied.

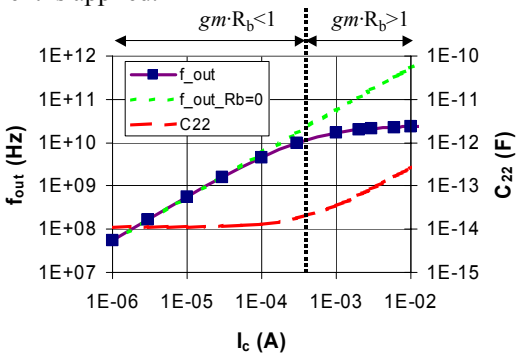

Fig. 4: Effect of the base series resistance R_b on the output capacitance C_{22} and bandwidth f_{out}.

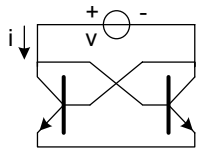

Fig. 5: Circuit to extract f_{cross}.

For the circuit of Fig. 1, f_{cross} equals

$$f_{cross} \approx f_T \sqrt{\frac{1}{gm \cdot R_b}} = \sqrt{f_V \cdot f_T} \qquad (4)$$

To obtain a high f_{cross}, a low base series resistance is essential.

For the SiGe process of [5], the device metrics across a bias sweep are shown in Fig. 6. The curves are valid for a 0.5x4.7 µm^2 npn transistor biased at $V_{cb} = 0$ V.

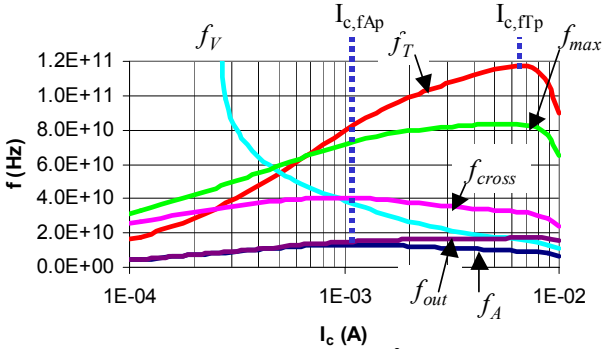

Fig. 6: Device metrics for a 0.5x4.7 µm^2 npn from [5].

From the curves shown in Fig. 6, some interesting observations can be made. Firstly, it can be seen that f_{cross} is relatively independent of the bias current for an order of magnitude in bias current variations. This can be explained from equation (4). For bias conditions below the current density for peak-f_T, the increase in f_T for increased bias current is compensated by a reduction in f_V. Secondly, from the crossing of the f_V and f_T curves follows that the condition $gm \cdot R_b = 1$ occurs at a current density well before peak-f_T. Thirdly, the current density for peak-f_A lays a factor of 5 below the current density for peak-f_T. This is due to the saturation of f_{out} for currents where $gm \cdot R_b$ becomes larger than unity. At peak-f_A, the f_A is dominated by the output bandwidth f_{out}. Such information is important for circuit design. A differential pair amplifier biased at peak-f_T may not provide the maximum bandwidth in this process.

III. EVOLUTION OF THE DEVICE METRICS

In Table I, the evolution of the device metrics across 3 generations of a 0.25 µm BiCMOS process are shown for V_{cb} = 0 V. The table refers to values obtained from Spectre circuit simulations. The last column is extracted from the f_T/f_V-ratio at peak-f_T, which provides a good approximation for $gm \cdot R_b$ as follows from equation (1).

Process	Year	f_T GHz	f_{max} GHz	f_A GHz	f_{cross} GHz	$gm \cdot R_b$ at pkf_T
[3]	2001	33	60	14.6	27	1.7
[4]	2002	61	73	15.2	34	2.3
[5]a	2004	117	84	13.0	40	5.9
[5]b	2004	109	90	15.9	47	5.0
[5]c	2005	108	117	24	62	2.8

Table I: Evolution of device metrics (peak values).

The transition from [3] to [4] was driven by an increase in peak-f_T, made possible through the introduction of a SiGe layer. The higher peak-f_T is obtained at an increased current density. The base series resistance R_b remained constant. This resulted in an increased $gm \cdot Rb$ at peak-f_T, and thus a more dominant effect of the output bandwidth to f_A due to the Miller effect in C_{bc} as follows from equation (2). Process [5] is currently still under development. In Table I the processes [5]a, [5]b and [5]c represent three stages in the process development. In the initial stage [5]a the maximum f_T was increased, mainly by the introduction of carbon into the base, which inhibits boron diffusion. The accompanied increase in base- and collector doping resulted in an increased base-collector capacitance C_{bc}. In combination with an approximately constant R_b (dominated by the extrinsic part), this resulted in a reduction of the output bandwidth f_{out}, explaining the reduced f_A in [5]a, despite the increased f_T and f_{max}. In a second step ([5]b), process spreading was reduced, which allows a narrower emitter and consequently a higher f_{max} and f_A. In a third step ([5]c), the base resistance was further reduced by about a factor of two.

For process variants [3], [4] and [5]a, the peak-f_A occurs at an approximately constant current density (where $gm \cdot R_b \approx 1$ to 2), and thus the ratio between the current densities for peak-f_T versus peak-f_A increased when migrating from [3] to [5]a. This is an undesired effect, since differential pair amplifiers operated at peak-f_T have a reduced bandwidth in the newer generation, despite the increase in f_T and f_{max}. The reduction of R_b by a factor of two in [5]c shifts the saturation of f_{out} to higher currents resulting in a substantially increased peak-f_A and f_{cross}. In a final step, f_T and f_{max} were further increased to values around 130 GHz without compromising f_A and f_{cross}. For these results, no parameters are available yet and therefore this process step has not been included in Table I. The increase in f_A and f_{cross} is reflected in broadband circuit performance, as demonstrated in the next section.

IV. CIRCUIT EXAMPLES

Metric f_A is defined for a low-frequency gain of 20 dB. Such a high gain is not widely used, and puts extra emphasis on the output bandwidth of a transistor. For example, bipolar current-mode logic (CML) circuits typically operate at a small-signal gain of 6 to 12 dB. The extra emphasis on the output bandwidth accounts for loading effects, which is necessary since in the definition of f_A, the output is unloaded. Note that circuit bandwidths may also exceed f_A.

Circuit simulations and measurements revealed only a minor increase in the maximum operation frequency of a static CML frequency divider, from 20 GHz in [3] (see [6]) to about 25 GHz in [4] (see [7]). The circuit was recently processed in [5]c, and operated up to 40 GHz. The maximum operating frequency of the divider is proportional to the peak-f_A. All 3 circuits support input frequencies up to approximately $1.5 \cdot f_A$. The same conclusion was found during the design of a cross-connect switch for optical networking applications [8]. The design was implemented in [4] since this process features two thick top interconnect layers, needed for low-loss transmission lines for rows and columns in the cross-connect matrix. In every signal path through the matrix, about 10 differential pair amplifiers are cascaded. The circuit supports input data rates up to f_A.

The next circuit example deals about a pseudo-random binary sequence (PRBS) generator in an InP HBT process [9]. This process has a peak-f_A of approximately 25 GHz. Our PRBS generator implemented in this process [10], based on CML circuits, supports output bit rates up to about $2 \cdot f_A$. Due to the half-rate architecture, the majority of the circuits operate at f_A, except for the output multiplexer and buffer, which operate at $2 \cdot f_A$.

For LC-VCO design, metric f_{cross} is valuable. An LC-VCO can be implemented for output frequencies close to f_{cross} [2]. A capacitively loaded emitter follower allows the implementation of a negative resistance that is feasible at frequencies beyond f_{cross}. Such a topology is also used in a Colpitts oscillator. This topology does not lead to different requirements to the transistor compared to the requirements for high f_{cross}.

V. CMOS VERSUS BIPOLAR

For CMOS, f_A is dominated by f_{out} since the transistor layout can be optimized for very low gate series resistance R_g and thus high f_V, (e.g., f_V > 100 GHz is often feasible). When comparing bipolar versus CMOS, a CMOS process with comparable f_T and f_{max} may possess a relatively poor f_A, as shown in Table II, where a 0.12 µm CMOS process is compared with the SiGe BiCMOS process from [4]. Despite the favorable f_T and f_{max}, the f_A is substantially lower in the CMOS process. This is due to the relatively low transconductance, requiring high load resistance values that reduce the output bandwidth.

Process	f_T (GHz)	f_{max} (GHz)	f_A (GHz)	f_{cross} (GHz)
CMOS12	86	138	6.7	123
[4]	61	73	15.2	34

Table II : Example CMOS metrics, compared with a bipolar process with somewhat lower f_T and f_{max}.

Furthermore, the higher impedance level in CMOS technology makes the impact of interconnect parasitic capacitances more important, and thus it is more difficult to realize circuit bandwidths predicted by f_A.

For CMOS, the favorable f_V also results in a favorable f_{cross}. Thus, the realization of microwave LC-VCOs in CMOS is usually not a problem, even in relatively outdated process generations. This statement is supported by a 38.7-41.8 GHz VCO that was implemented in 0.18 µm CMOS with f_{cross} > 100 GHz. The chip photomicrograph is shown in Fig. 7, the output spectrum at 40 GHz shown in Fig. 8.

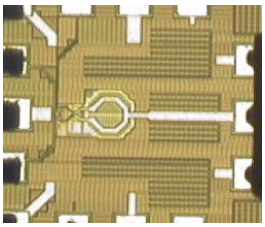

Fig. 7: 40 GHz LC-VCO in 0.18µm CMOS.

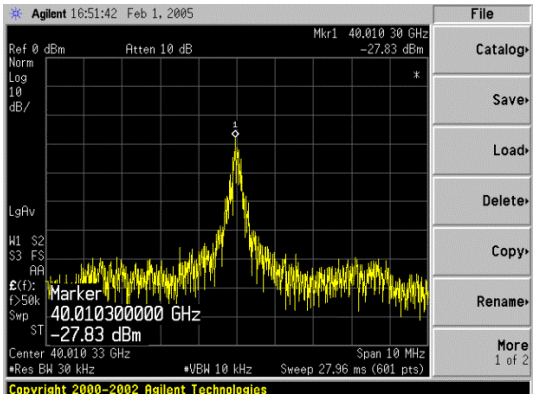

Fig. 8: Measured output spectrum at 40 GHz.

The relatively low oscillator output power is due to the –23 dB voltage gain of differential pair output buffer, driving the external 50 Ω load. This confirms that signal distribution and frequency division are more a challenge than signal generation in CMOS.

VI. Conclusion

The available bandwidth f_A, representing the 3-dB bandwidth of a differential pair amplifier designed for 20 dB low-frequency voltage gain, is a valuable performance indicator for broadband circuit applications. A technology with superior f_T and f_{max} may have a lower f_A, and therefore not show the expected speed advantage. Metric f_A can be subdivided into two contributions: the input bandwidth f_V and output bandwidth f_{out}. Since IC processes are typically designed to allow current densities up to operation for peak-f_T, it is important to avoid saturation of f_{out} up to such current densities. If this can be realized, the current density for peak-f_A will be close to the current density for peak-f_T. For a given technology, analyzing f_V, f_{out} and f_T across a bias sweep provides information about the main limiting factor to f_A, and shows whether the IC process is well balanced between in- and output bandwidths. The output bandwidth saturates for current levels above $gm \cdot R_b = 1$ due to the Miller effect of C_{bc}. The bias point where $gm \cdot R_b = 1$ corresponds to the crossing of the f_V and f_T curves. Broadband circuits are demonstrated that support data rates up to f_A (for a complex cross-connect switch) up to $2 \cdot f_A$ (for CML frequency divider and PRBS generator).

A CMOS transistor can be designed for very low gate series resistance, thereby achieving an extremely high input bandwidth f_V. Thus, f_A is dominated by the output bandwidth f_{out}. The high f_V also results in a relatively high f_{cross}, even for mature CMOS processes. Thus, microwave VCOs can be implemented in mature CMOS technologies (as demonstrated), but the performance of CMOS processes with favorable f_T and f_{max} for broadband circuit design does not yet reach the capabilities of BiCMOS due to a relatively poor gm and f_A.

Based on our experience, we evaluate IC processes on the basis of f_T, f_A and f_{cross} rather than f_T and f_{max}.

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