# Partially Depleted CMOS SOI Technology for Low Power RF Applications

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***Abstract* — The low resistivity substrate that is used in bulk silicon processes (CMOS and BiCMOS) limits the integration of high-quality passives components and gives rise to severe substrate coupling issues. This paper will show how to take advantage of HR SOI to improve RF circuit performances as well as the effectiveness of HR SOI to reduce substrate coupling. Potentiality of mm-wave passive integration is also shown.**

## I. Introduction

The continuous scaling down of CMOS technologies has allowed operation in the gigahertz region, then providing the opportunity for low-cost integration of RF/digital/analog functions on the same chip. On the other hand, high level RF-digital baseband integrations in silicon technologies are mainly limited by the severe substrate coupling issues introduced by the low resistivity of classical silicon substrates. Indeed in the past, in order to improve passive devices performances at RF frequencies and limit substrate coupling, CMOS technologies have already migrated from the very low resistivity substrates (0.01 Ω·cm), originally used for VLSI, to medium resistivity substrates (~15-20 Ω·cm), used in RFCMOS and BiCMOS. However, this migration has only slightly mitigated substrate coupling and the shift to higher resistivity substrates will lead to high latch-up susceptibility if state of the art digital integration and low cost process shall be preserved.

SOI technologies offer the opportunity to marry VLSI CMOS process and substrates with a resistivity above 1 KΩ·cm, boosting further passives RF performances and substrate coupling robustness without loosing an intrinsic latch-up immunity. As shown in this paper, the result is a technology able to provide excellent RF properties with the historical 20% digital power saving over classical CMOS working at the same frequency [1]. Furthermore, it is worth noting that SOI high resistivity substrates allow the integration of good passive up to 60 GHz. This asset, coupled with the potentiality of last generation MOSFETs providing $f_{MAX}$ over 250 GHz [2], pushes CMOS into the mm-wave integration age.

## II. High Performance Integrated Passives

Taking advantage of high resistivity (HR) substrates in SOI, some recent works [3] at STMicroelectronics (Crolles) have investigated the realization of high-quality passives in SOI HR.

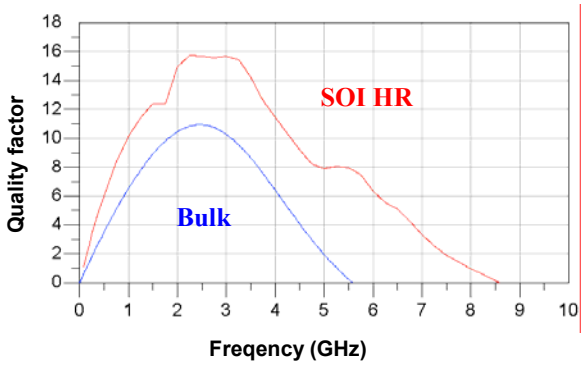


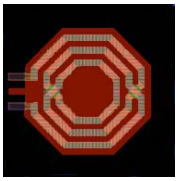

Fig. 1. Q factor of 3.4nH inductor optimized for 2.45 GHz[3]

The impact of substrate resistivity, and benchmarking with standard bulk process, on key components of RF CMOS for SOC is presented hereafter. The comparison includes inductor and transmission lines.

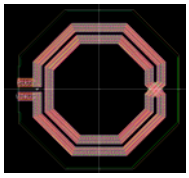
In standard bulk processes, the highest-Q inductors are achieved over a Patterned Ground Shield (PGS) to limit the losses in the substrate. In SOI, the opportunity to use high-ohmic substrates (ρ>1000 Ω.cm) allows to avoid this PGS. As a consequence, better quality factor (Q) can be achieved as it is demonstrated Fig.1. But if one only retires the PGS, the increase in performance will occur at higher frequencies, which would generally not improved a design since the inductor are optimized to resonate at the operating frequency of the circuit. Nevertheless, if we make a specific layout of the inductor in order to use differently the modification of the parasitic capacitance, we can achieve 50 % gain on the inductor Q at the operating frequency as it is shown Fig.1.

To obtain this increase of performance at a given frequency, cautious attention has to be given to the way the layout is done. The goal is to take advantage of the reduced parasitic capacitance on SOI HR to use wider conductor and then decrease DC resistance. The layout of the inductors compared Fig. 1 can be found Fig. 2.

Moreover, today CMOS 90 nm cut-off frequencies are higher than 150 GHz [2] and this increase allows new millimetre wave applications on silicon such as 60 GHz WLAN and 77 GHz automotive radar. As a consequence, transmission lines performance would have a key impact on the feasibility of such applications in silicon technology, since at these frequencies the use of distributed element is prefered to realize passive network.



« bulk » inductor



SOI HR inductor

Fig. 2. Layout of bulk and SOI HR optimized 3.4 nH inductor [3].

In order to investigate millimetre wave performance of SOI technology, we have realized and measured coplanar transmission line (CPW), in SOI HR. A cross section can be found Fig.3. Measurements have been performed on wafer up to 80 GHz using an Agilent HP8510XF vector network analyzer.

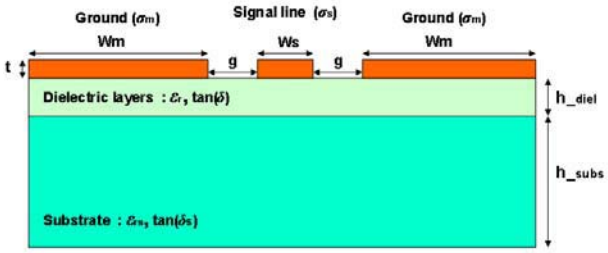



Fig. 3. Coplanar transmission line structure.

Results are impressive, for 50 Ohms characteristic impedance, loss better than 0.5 dB/mm at 40 GHz and 1 dB/mm at 80 GHz have been measured (Fig.3). With such performance, integrated passive components in SOI HR could be compared with InP [4] or other insulating technologies. That is what we have illustrated in the benchmarking proposed Fig.4.

## III. Substrate Coupling Issue, What Does SOI Change?

The coupling through the substrate is another important limiting factor in mixed-mode high-frequency integrated circuits. Since analog parts are very sensitive to voltage variation of power suppliers as well as of the substrate ground, painful attention should be given to the isolation with digital parts, their strong and sudden signal switching. If not, noise is transmitted to the analog part lying on the same chip, causing a degradation of its performances. First study [3] demonstrated a potential advantage of standard SOI substrates versus bulk for cross talk reduction for frequency up to 1 GHz.

A second one investigates the use of very high-resistivity SOI substrates as recommended for very high-frequency or microwave applications [5]. We have used the same type of simple test structure (we measured the isolation between two P+ implants) to evaluate the gain in term of isolation provided by SOI HR. It can be seen Fig.5. that a gain in the order of 10 dB can be obtained using SOI HR in comparison with standard bulk process. In this section we show how to take advantage of HR SOI to improve RF circuit performances. We present results on a few RF blocks which have been optimised: 5GHz VCO, a 5GHz LNA and a low pass antenna switch.

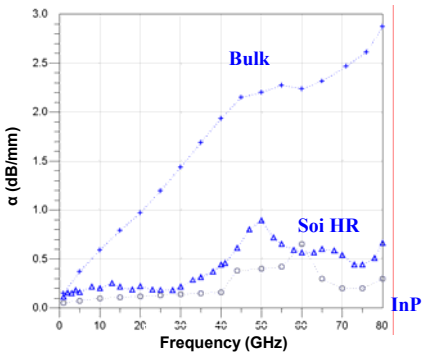



Fig. 4. Losses for coplanar wave guides – Bulk vs. HR SOI and InP.

As a consequence, from coupling reduction point of view, SOI HR technology could make feasible the realization of SOC dedicated to communication system in the 1-10 GHz band using a compatible simple CMOS process. Moreover, additional studies have demonstrated that the situation can still be improved if using guard ring.

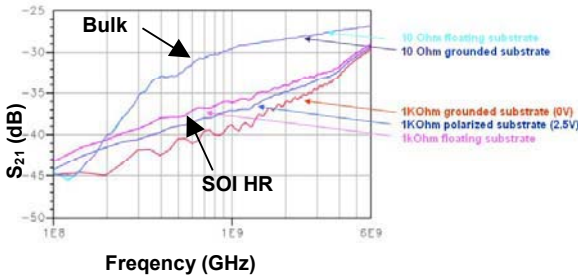



Fig. 5. Measurement of isolation – Bulk vs. HR SOI [1].

## III. Circuit Implementations

### *A. 5 GHz SOI optimized VCO*

One of the most power-hungry RF blocks in a wireless transceiver is the Voltage-controlled-Oscillator (VCO). In a cross-coupled LC-tank VCO, the degradation of the phase noise performance due to the varactors is minimized by using a bank of switched varactors for the coarse tuning and a single one for the fine control inside the Phase-Locked-Loop (fig. 6 (a)). The other contributor to the tank losses, the inductor, has to be carefully optimized.

The inductor could be optimized thanks to HR SOI to offer an increase of Q at the operating frequency. With the same layout as in bulk, a gain of 3 in Q for the 2nH inductor is achieved while an optimized layout allows getting a gain greater than 6, near 50%. In the LC-tank VCO of Fig. 6 (a), the inductor is driven by a differential signal. To have a fair comparison at the circuit level, we have to consider the differential Q. The inductors on PGS and HR have then been modelled with a classical Π model and they have been slightly tuned to have their maximum differential Q at 5 GHz. The gain in Q is now equal to 10, or near 60%.

The VCO was then optimized for these two inductors. The inductor improvement on HR allows not only reducing the contribution to phase noise from the tank but also reducing the contribution from the transistors,

shrinking them proportionally to the reduction of tank losses. A comparison using Hajimiri phase noise model [6] is presented in Fig 8.

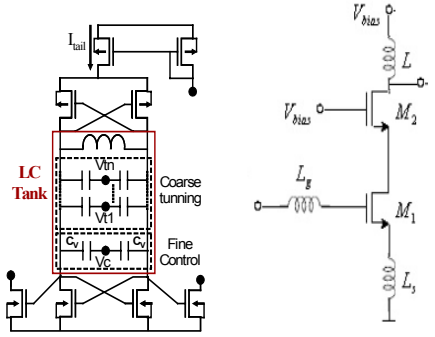



Fig. 6. a) LC-VCO with coarse tuning & fine control
b) 5GHz LNA schematic.

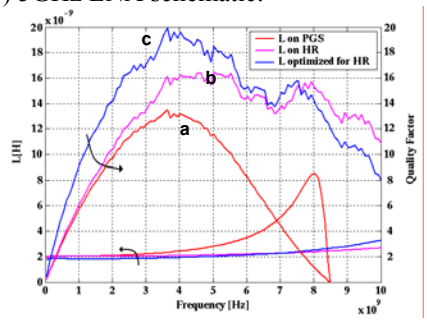



Fig. 7. Measurements of a 2nH inductor and its quality factor (Q) versus frequency on a PGS (a), on a HR SOI substrate with the same layout (b) and with optimized layout (c).

The VCO was then optimized for these two inductors. The inductor improvement on HR allows not only reducing the contribution to phase noise from the tank but also reducing the contribution from the transistors, shrinking them proportionally to the reduction of tank losses. A comparison using Hajimiri phase noise model [6] is presented in Fig 8. A 4.2 dB reduction of the phase noise, i.e. 60%, is obtained and for a constant phase noise of -126 dBc at a 1 MHz offset, the current consumption is reduced from 2.6mA down to 1.6mA. The 5GHz VCO has been designed using thick gate oxide transistors (tox=5 nm), N-type accumulation-mode varactors with a Q in excess of 200 at 1GHz and with the best inductor of Fig. 7. Phase noise measurements and the FoM versus the tail current are presented in Fig. 8 and 9 respectively. Because a precise model of the inductor was not available at the time of the design, a not so high Q was expected for the tank and a conservative optimization was done. A further optimization is expected to give even better results. However, FoM at the top of the state-of-the-art, -190.4 at 4.6GHz and -188.6 at 5.84GHz, as well as very low power consumption have been obtained (Table 1).

### *B. 5 GHz SOI optimized LNA for WLAN application*

In RF transceiver, antenna is always followed by a low noise amplifier (LNA). Indeed, this circuit is mandatory to avoid a degradation of signal to noise ratio by analog signal processing (e.g. filtering and mixing) needed before analog to digital conversion. Figure 6 (b) shows the schematic of the designed LNA, commonly called cascode with inductive source degeneration [7]. This is a widespread structure which uses many inductors and therefore takes great advantage of the inductor quality factor improvement brought by HR SOI. To evaluate the impact of the enhanced SOI inductors the same LNA has been designed with bulk and SOI passive models: transistor`s size is unchanged while inductors value and layout have been optimized for each technology. For both LNA versions (SOI and bulk) Fig. 10 and fig. 11 compare simulated gain and noise figure respectively, which are the main block figures of merit. The performances enhancement thanks to the increased inductors Q is clear: for a fixed power consumption of 6mA @1.2V, power supply gain and noise figure are improved with the HR SOI by 2 dB and 0.4 dB respectively.

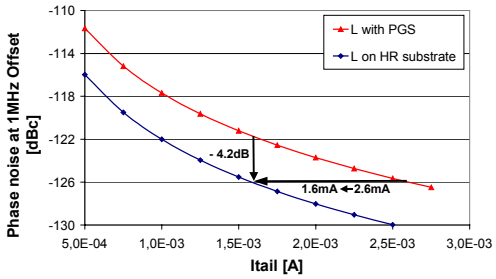



Fig. 8. Phase noise improvement with HR SOI.

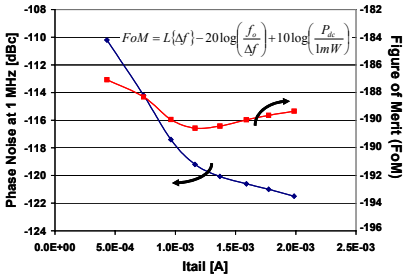



Fig. 9. Measured phase noise and FoM on the 5GHz VCO with HR SOI.

### *C. Integrated antenna switch*

Most of the wireless standards (Bluetooth, WLAN, GSM…) employ time-division duplexing (TDD) as a way to share the same antenna between the receiver and the transmitter. In these systems, antenna switch is a key RF component. Recently, several attempts [8-10] have been made to integrate this function in CMOS technologies, especially for low power TX applications as Bluetooth and WLANs. However, despite the good trade-off reached beetwen loss and power handling, in all these previous works, due to the substrate coupling, isolation rapidly degrades above 2.5 GHz giving, in the best case, only 30 dB in the range 5.2-5.8 GHz. Fig. 12 shows the measured results we obtained with a Single Pole Double Throw antenna switch integrated in a 0.13µm CMOS SOI process using high resistivity substrate. The antenna switch has been integrated in an asymmetric way to optimize isolation in the TX mode and loss in the RX mode. Clearly in the TX mode, which is the more critical mode, the use of high resistivity allows to strongly reduce substrate coupling leading to an isolation of more than 40 dB at 5 GHz. On the other hand it is worthwhile to highlight that in this case

| Ref. | f0 [GHz] | L{1 MHz} [dBc/Hz] | VDD [V] | Tuning Range | P dc [mW] | FoM [dBc/Hz] | Technology | Comments |
|---|---|---|---|---|---|---|---|---|
| Samori [11] | 4.2<br>5.05 | -114<br>$f_c$ = 5 GHz | 2.5 | 18 %<br>(2.5 V) | 13.8 | - 176.6 | 0.25 µm<br>Bulk | AMOS<br>Varactors |
| Magret [12] | 3.28<br>4.11 | -117<br>$f_c$ = 4 GHz | 2.5 | 33 %<br>(2.5 V) | 7.5 | - 180.2 | 0.25 µm<br>Bulk | AMOS<br>Varactors |
| Svelto [13] | 1.8<br>2.45 | -125<br>$f_c$ = 1.9 GHz | 2.0 | 26.5 %<br>(4 V) | 2.0 | -187.6 | 0.35 µm<br>Bulk | High Tuning<br>Voltag |
| Kucera [14] | 1.75<br>2.51 | -134<br>$f_c$ = 1.9 GHz | 2.7 | 35.7 %<br>(2.7 V) | 12.2 | -189.4 | 0.25 µm<br>BiCMOS | Bonwire<br>inductor |
| Fong [15] | 3.065<br>5.612 | -120.8<br>-114.6 | 1.0 | 58.7 %<br>(1.4 V) | 3.0<br>2.0 | -185.6<br>-186.6 | 0.13 µm<br>PD SOI | AMOS |
| This work | 4.6<br>5.84 | -120<br>-116 | 1.4 | 24.8%<br>(2.4V) | 1.92<br>1.69 | -190.4<br>-188.6 | 0.13 µm<br>PD SOI | AMOS<br>GO2 & HR |

TABLE I
VCOs Performances: State of the art

good isolation performances have been reached keeping loss low, below 0.9 dB up to 6 GHz.

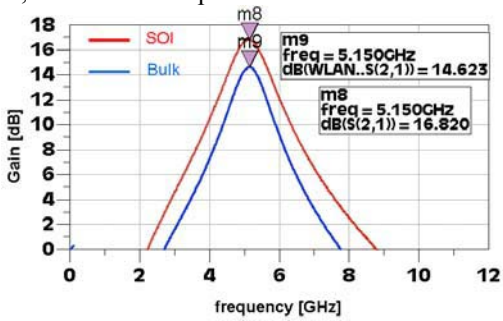



Fig. 10. Noise Figure of the simulated LNA, bulk vs. SOI HR.

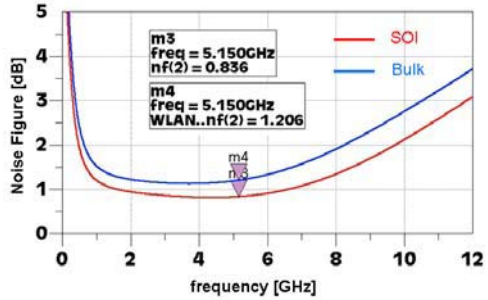



Fig. 11. Noise Figure of the simulated LNA, bulk vs. SOI HR.

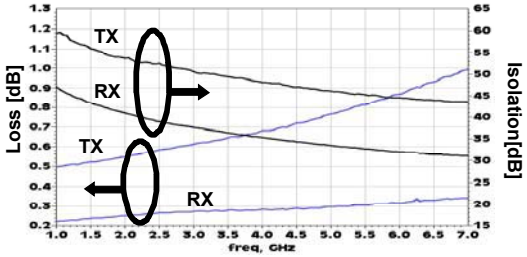



Fig. 12. Measured Isolation and loss of TX/RX antenna switch.

## VI. Conclusion

This paper shows how the use of CMOS SOI technology coupled with high resistivity substrates strongly improves RF behaviour of passive devices compared to classical bulk technologies (CMOS and BiCMOS), where latch up risk does not allow the use of high resistivity substrates. Such passive improvement leads to an effective power saving in the main RF blocks (LNA, VCO) for fixed circuit`s performances and is preserved up to 60 GHz making feasible CMOS design at mm-wave frequencies. Furthermore, thanks to the very low substrate parasitics affecting SOI active devices, antenna switches become feasible with very good loss-isolation-power handling trade off.

Finally, such a good isolation shows that CMOS HR SOI technology has a great potential to deal successfully with substrate coupling, which is the main troublemaker affecting highly integrated RF systems, where digital and analog/RF circuits are integrated on the same chip and weak analog signal must be protected from noisy digital signals.

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