Wideband characterization and simulation of advanced MOS devices for RF applications

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Abstract — Multiple-gate SOI MOSFETs are potential candidates for achieving the performance expectations of the International Roadmap of the Semiconductor Industry Association. In this paper, experimental and simulation analyses have been carried out to compare the analog/RF performance of single and multi-gates SOI MOSFETs using the commercially available 3-D numerical simulator, SILVACO. Their characteristics were analyzed in DC and AC regimes from subthreshold region to strong inversion and saturation region. In both regimes, the advantages and limitations of the multiple-gate devices over the single gate structure with channel length scaling well below 100 nm are discussed for high frequency analog applications.

I. Introduction

It is widely known that in the next decade, the continuation of the Moore's scaling law according to the International Technology Roadmap for Semiconductors (ITRS) [1], below the 45 nm node, is facing many considerable technological difficulties, among which short channel effects (SCE) in Single-Gate (SG) MOS structures, despite the deployment of channel and gate engineering [2]. Even, in ultra-thin-film SOI technology, results have shown that the transconductance and AC characteristics for gate lengths down to 40 nm are deteriorated due to SCE [3]. Multiple-gate MOSFETs then emerge as one of the most promising novel device structures to solve the SCE problem, thanks to the simultaneous control of the channel by more than one gate. Several types of multi-gates (MG) devices have been proposed in the literature these last years such as Triple-Gate (TG), FinFET, Pi-Gate (PG), Quadruple-Gate (QG), Omega-Gate (Ω-G), etc. [4-6]. Some early research in the subthreshold region demonstrated the great potential of these MG devices to comply with the I_{on}/I_{off} requirements of the ITRS for logic operation [5].

In the present paper, we focus our analysis on the analog and RF behaviors of the multiple-gate devices. In the ITRS for RF and Analog/Mixed-signal Technologies, the main figures of merit are the gate oxide thickness (t_{ox}, always slightly thicker that the one for logic at the same node), the intrinsic gain or transconductance to drain conductance ratio (g_m/g_{ds}), the cut-off frequency (f_T) and the parasitic capacitances. In the present work, results from simulation and measurements of multiple-gate devices will be analyzed and compared with regards to these ITRS target performances.

II. Experimental Data

The experimental devices available for our analog/RF analyses were FinFETs processed at IMEC, Leuven, Belgium and featured (Fig. 1):

- either fixed fin width W_{fin} = 33 nm with gate lengths L from 10 µm to 50 nm and fin height H_{fin} = 75 nm.
- fixed L= 10 µm with various W_{fin} varied from 10 µm down to 35 nm and H_{fin} = 95 nm.
- or finally, embedded in coplanar feed lines for RF measurements with L = 50 nm, W_{fin} = 50 nm, H_{fin} = 75 nm and fin spacing (S_{fin}) = 100 nm.

All of these devices have a nitrided gate oxide of 2 nm equivalent oxide thickness (EOT), high angle extension implantation of As+P and B deep source/drain with the presence of 70 nm RTCVD nitride spacers. NiSi was used as a salicide and the p-type channel doping was of 10^{18} cm^{-3}.

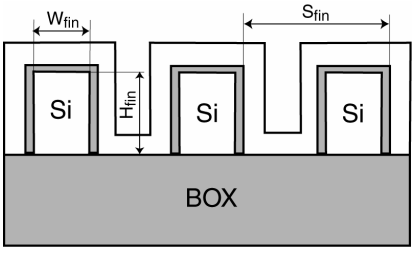

Fig. 1. Cross-section of FinFETs channel.

The assessment of their analog performance was performed according to the methodology we presented in [7]. The intrinsic gain (g_m/g_d) is decomposed as $g_m/I_{ds}xI_{ds}/g_d$. The transconductance to current ratio (g_m/I_{ds}) is an important parameter for the design of analog circuits as it shows the effectiveness of the device in generating the transconductance which relates to the ability of the MOSFET device to amplify a signal under a certain power dissipation (I_{ds}) [8]. This figure of merit is then important as it represents the efficiency of the device to convert DC power into AC frequency and gain performance. When represented as a function of the normalized current $I_{ds}/(W/L)$ where W is the gate width, g_m/I_{ds} presents the additional property to become independent on the threshold voltage and device length (as long as SCE are negligible). The Early voltage V_{EA} (= I_{ds}/g_d) has been chosen to represent the output conductance g_d in order to avoid the dependence of g_d on I_{ds} and emphasize its length dependence.

Fig. 2 shows the $I_{ds}/(W/L)$ measured at a given g_m/I_{ds} on FinFETs with L = 10 µm, various W_{fin} and V_{ds} = 1.0 V.

Here, the W used for normalization depends on whether the device was Fully Depleted (FD) or Partially Depleted (PD). For FD devices, $W = 2\times H_{fin} + W_{fin}$ and for PD device, $W = 2\times H_{fin.}$ A dramatic increase of the normalized drive current by a factor larger than 2 appears for the narrowest FinFETs. This can be attributed to the VI [9]. As W_{fin} increases, the devices shift from FD to PD, the normalized current indeed reduces as a result of larger body effect and lower effective mobility. The increase of the current drive when W_{fin} is very large could be attributed to the improvement in the electrons mobility of the device thanks to the transfer of conduction from lateral (<110> crystalline plane) to top channel conduction (<100>).

Fig. 3 shows the dependence of V_{EA} versus W_{fin} at V_{gs} = 0.5 V and V_{ds} = 1.0 V for 10 µm long FinFETs. For large W_{fin}, the devices operate as PD devices and thus, the output conductance in saturation is deteriorated by the kink effect. As W_{fin} decreases, the devices move towards the FD region, the kink effect is suppressed and V_{EA} improves. For the narrowest fins, V_{EA} is strongly increased to values on the order of 100 V per µm of channel length. According to [10], such high V_{EA} values have only been experienced in devices operating in VI.

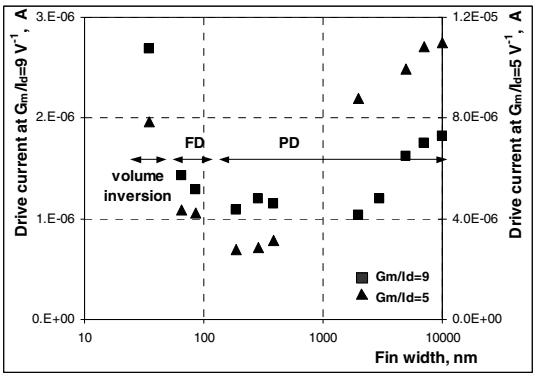

Fig. 2. Dependence of the fin width with normalized current drive at V_{ds} = 1.0 V for L = 10 µm.

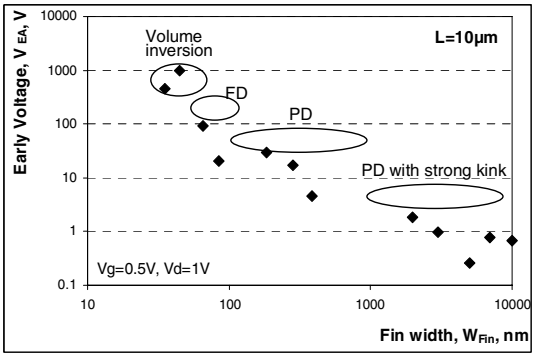

Fig. 3. Early voltage for FinFETs with different width V_{gs} = 0.5V and V_{ds} = 1.0 V and L = 10 µm.

In order to confirm and interpret these experiments in depth, in particular the role of VI, numerical device simulations are performed in next section.

III. Device Simulations

3-D numerical simulations have been performed for planar DG, TG/FinFET, Pi-Gate and SG SOI MOSFETs using Silvaco Atlas numerical simulator. The dimensions of the DG, TG/FinFET, PG and SG simulated devices were chosen according to the analog/RF ITRS 45 nm node parameters: silicon film thickness (t_{Si} or W_{fin}) = 20 nm, gate oxide thickness (t_{ox}) = 2 nm and buried oxide thickness (t_{box}) = 150 nm. The channel doping level is $10^{15}cm^{-3}$ and the gate electrode workfunction set to 4.67 eV which corresponds to Molybdenum [11] to get an adequate long-channel threshold voltage of 0.3-0.4 V for all devices. The channel length was varied from 25 nm to 500 nm. The corresponding width ($W = 2 \times H_{fin} + W_{fin}$) used for the TG and PG was 120 nm, with H_{fin} (= 50 nm) and W_{fin} (= 20 nm). For the PG device, an extension of 20 nm of the gate vertically into the buried oxide was considered, since demonstrated sufficient for strongly reducing the SCE in [6]. In order to take into account all the parasitic capacitances of the transistors 3-D structure the source, drain and gate connections were introduced. The physical models that have been used in the simulations accounted for the electric field dependent lifetime, transverse field dependent mobility, bandgap narrowing, SRH recombination/generation, and carrier statistics. The SG devices was not optimized i.e. no channel or gate engineering technology was implemented to allow a comparison of the intrinsic performance with the other devices. The results of DC simulations presented in [12] demonstrated that V_{th} roll-off and S and DIBL degradations were acceptable for all multiple-gate devices down to L = 50 nm, whereas only L = 75 nm for the SG. For the analysis in the AC regime, a small signal frequency from 1 MHz to 200 GHz with an amplitude of 30 mV was applied.

A. DC Analysis

As mentioned earlier, the main advantages of using multiple-gate devices for high analog performance is suspected to be related to VI. Here, this effect will be simulated for the DG SOI MOS structure. Device simulation will furthermore allow us to separate the influences of the improved body factor and effective mobility which were combined and indistinguishable in the measurements. Fig. 4 shows the simulated g_m/I_{ds} ratio dependence on the normalized drain current at V_{ds} = 1.0 V. It is clear that the DG structure results in higher g_m/I_{ds} values compared to the SG structure. The excellent g_m/I_{ds} value of nearly 38 V^{-1} in the weak inversion region is related to a near ideal value of the S (= ln (10)/(g_m/I_{ds}) = 60 mV/dec) for $L \geq 100$ nm.

In Fig. 5, the extracted mobility (µ) and electron concentration (n_s) at the surface and the center of the silicon film ($t_{Si}/2$) for L = 100 nm DG SOI MOS at V_{ds} = 1.0 V is shown. At low V_{gs}, the carriers tend to spread out across the silicon film, which indicates the presence of the VI because here, the potential and the electron concentration at the center and at the surface of the film are equal. As V_{gs} increases, the carriers at the surface will have a screening effect on the carriers at the center of the film, therefore this causes the potential at the center of the film to remain the same while the potential at the surface increases due to the increase of V_{gs}. Due to this imbalance of the potential, the increase rate of n_s will be

much higher at the surface compared to the center of the film. Another phenomenon that happens at high V_{gs} is the domination of the surface mobility compared to the mobility of the carriers in the center of the film even though there is a reduction of the vertical electric field on the carriers at the center. Thus, it is obvious that there is a shift of the importance of the mobility mechanism from weak inversion (low V_{gs}) to inversion and strong inversion region (high V_{gs}) where the role of the dominant carriers with relation to the mobility is shifted from the center to the surface of the film. In the strong inversion region, DG will behave as a dual operating channel device and the I_{dsDG}/I_{dsSG} will tend to a ratio of 2.

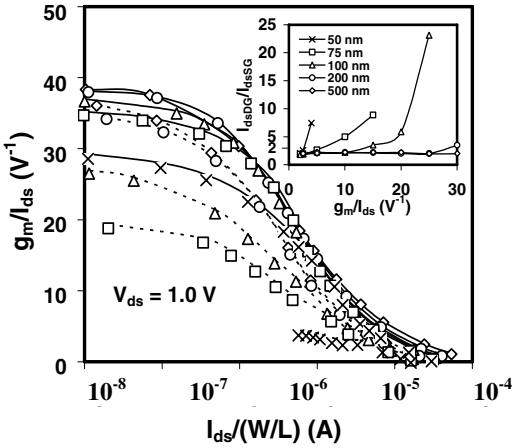

Fig. 4. g_m/I_{ds} for DG and SG devices with normalized drain current at V_{ds} = 1.0 V (DG —, SG ---, × 50 nm, 75 nm, Δ 100 nm, o 200 nm, ◊ 500 nm).

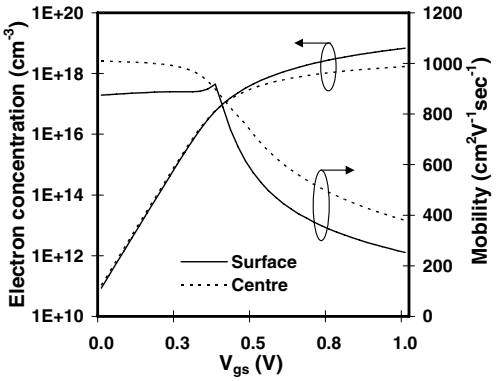

Fig. 5. Electron concentration and mobility simulated at $x = L/2$ at 1 nm below the surface and center of DG MOSFET at V_{ds} = 1.0 V and L = 100 nm.

Fig. 6 shows the V_{EA} for L = 50 nm at V_{ds} = 1.0 V, where again we see that the DG, TG and PG devices are able to generate higher V_{EA} compared to the SG structure.

From the measured (Fig. 2, 3) and simulated (Fig. 4, 6) results, we have been able to show that multiple-gate devices will be able to achieve the required g_m/g_{ds} @$5_{\cdot Lmin\text{-}digital}$ = 100 as laid out in the ITRS for the 45 nm node. At this node, the simulations and measured devices show a g_m/g_{ds} > 100, with values reaching 480 and 318 for the DG and TG devices, respectively. Again, these improvements for MG devices are linked to the improved control of the charges and the VI. The good controllability of the multiple-gate devices on the charges due to the reduced influence of the drain potential on the channel leads to an overall increase in the voltage gain compared to the SG device. Multiple-gate devices are also able to satisfy the criteria for higher current drive with stable V_{th} in the ITRS.

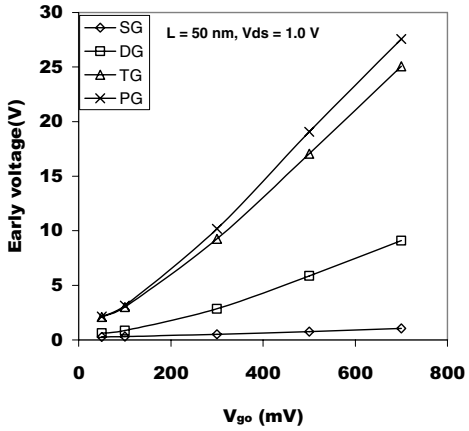

Fig. 6. Early voltage for MG and SG devices simulated at V_{ds} = 1.0 V for L = 50 nm.

B. AC Analysis

In this paragraph we analyze the cutoff frequency $f_T = g_m/(2\pi(C_{gs}+C_{gd})$. We have already compared g_m for various MG, so let now analyze C_{gs} and C_{gd}. As shown in previous paragraph, g_m for MG is improved quite a lot thanks to VI. However, C_{gs}, C_{gd} and g_m being all of them linked to electron concentration in the channel, in the case of VI, the increase of g_m is balanced by an increase of the gate capacitances, leading to an unchanged f_T. Therefore, the only way to increase f_T is to increase C_{gs}/C_{gd}, i.e. to reduce the feedback capacitance C_{gd}.

Intrinsic capacitances - Fig. 7 shows that MG devices have a higher C_{gs}/C_{gd} ratio compared to the SG structure. An improvement in this ratio is attributed to the reduction of the SCE in the multiple-gate devices which translates to a reduction of the Miller capacitance especially as L reduces.

Parasitic capacitances - Fig. 8 shows the normalized C_{gs} for various multiple-gate devices at V_{ds} = 1.0 V for L = 200 nm at various V_{go}. It is obvious here that there is an increase in the capacitances in the following sequence, TG > DG > SG. This higher capacitance in both the TG and DG devices is related to the 3-D interconnection structure which contributes to an overall decrease in the cut-off frequency for longer L as shown in Fig. 9. Experimental results presented in [13] showed indeed the increase of parasitic capacitances for MG devices.

It is clear that as L is reduced, the f_T for MG devices increases while that for the SG device deteriorates (for L < 75 nm). Again, as aforementioned, this degradation is related to the increase of the SCE in the SG. However, it is worth noting that MG devices present also a saturation of the f_T values for L lower than approximately 40 nm. In order to overcome this saturation of f_T for the multiple-gate devices, some of the options available are to reduce

further the silicon film thickness and/or use a thinner equivalent gate oxide (EOT).

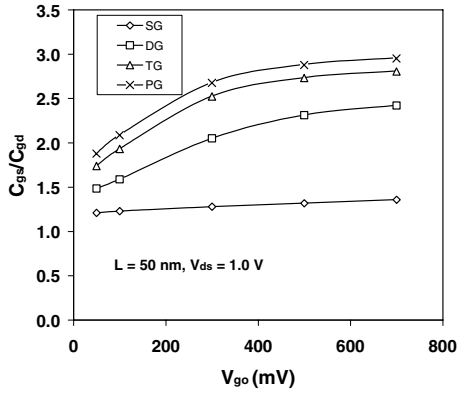

Fig. 7. C_{gs}/C_{gd} ratio for MG and SG devices extracted at V_{ds} = 1.0 V for L = 50 nm.

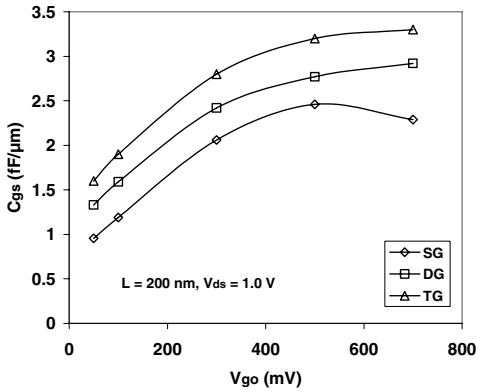

Fig. 8. C_{gs} for MG and SG devices extracted at V_{ds} = 1.0 V for L = 200 nm.

From the simulations, the extracted f_T values demonstrated by the DG, TG/FinFET and PG devices are extremely promising in moving the ITRS further. Values higher than 300 GHz could be reached with MG at the 25 nm node.

IV. Conclusion

In this paper, we have for the first time to our knowledge reported on the potential of multiple-gate compared to single-gate devices with regards to the analog/RF ITRS targets. In the static region, it is clear that multiple-gate devices have the edge over single-gate devices due to the advantage of the volume inversion effect.

The dynamic measurements and simulations in this paper have shown that moving into the 45 nm node, the advantages of using the multiple-gate structure will bring great improvement in the various figures of merit. From the simulations, it was also shown that for the multiple-gate devices, there is a limit in the characteristics when the gate length is reduced beyond the 25 nm node as there is an increase in the short channel effect. To benefit further beyond this node, there are 2 options available to reduce the short channel effect i) to thin down the channel silicon thickness, however, this will increase the access resistances of the source and drain, and therefore the use of optimized silicidation, localized silicon epitaxy or low Schottky barrier contacts will have to be considered or ii) to decrease the equivalent oxide thickness without increasing the gate leakage current via the use of high-k materials.

Further improvements on the analog performance of the MG devices could be obtained by optimizing the 3-D geometry of their intrinsic structure (channel) but also the interconnection. Indeed, for FinFETs, preliminary experimental and simulation results show that a higher aspect between fin width and height can contribute to the reduction of relative importance of parasitic capacitances. This increase of H_{fin}/W_{fin} ratio will also lead to an enhancement of the current drive per unit die area. Moreover, strained-Si technology for enhancing the carriers mobility for MG should be considered in a close future to fulfill the ITRS predictions for 25 nm node.

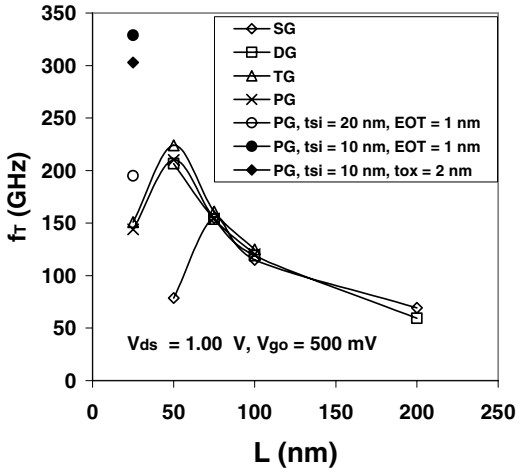

Fig. 9. f_T values versus L for various MG and SG devices extracted at V_{ds} = 1.0 V and V_{go} = 500 mV.

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