HIGH FREQUENCY CLASS E DESIGN METHODOLOGIES

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***Abstract* — Design criteria of Class E amplifiers are reviewed and extended for high frequency application. In particular, starting from classical Class-E formulas an additional tuning on fundamental output load becomes mandatory to take into account practical limitations arising in high frequency applications. Two examples of Class E amplifier designs for X-Band application (GaAs based) and C-Band (GaN based) are presented.**

I. INTRODUCTION

The design of high efficiency power amplifiers (PAs) is the designer's main challenge in a huge number of applications, especially in mobile or portable systems, due to the limited power supply accessibility. In this scenario, the output network choice represents the kernel of the overall design. In fact, while the input network is usually designed to assure maximum power transfer between the external source and the active device input, the output network has to be selected to maximize the drain efficiency, accounting for a device non-linear behaviour.

For radio frequency (RF) systems, the Class E strategy, published and patented by Sokal in the 70's [1], becomes a very interesting solution providing the highest theoretically and practically drain efficiency values achievable with a fixed active device. The Class E amplifier is based on the hypothesis that the active device is operated as a switch instead of the usual current source, either voltage (FET) or current (BJT) controlled. Its popularity is due to relative simple and closed form design relationships [2, 3] and robustness to circuit variations [4]. This is true especially for low frequency operation (i.e., few GHz and radio applications), demonstrating an efficiency record of 96% [5]. However, when increasing the operating frequencies, the active device can no longer be considered as an ideal switch due to parasitic effects practically shorting the higher frequency drain voltage components and increasing the switching time transitions that become not yet negligible. Therefore such limitations have to be accounted for to derive new useful and optimum design criteria.

In this paper, the classical Class E design approach will be briefly discussed in section II, while in section III the high frequency approach will be presented. Finally, in section IV two Class E PA designs, based on PHEMT and GaN devices, will be presented.

II. LOW FREQUENCY CLASS E DESIGN CRITERIA

Amplifiers designed according to Class E guidelines are based upon the idea that the active device acts as an ideal switch rather than an amplifier, and on the fact that the output network is designed to transfer active power on an external load only at fundamental operating frequency and ensures, at the same time, maximum drain efficiency performances. Even if several output network configuration are available [3], a common Class E PA configuration employs a single active device with the output network composed by a shunting capacitor C_1 and a series resonant filter C_S, L_S, as depicted in Fig. 1.

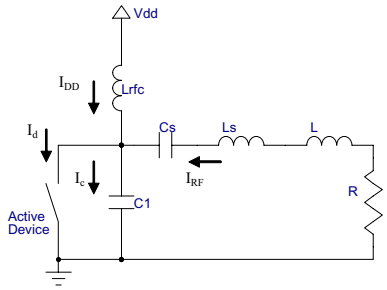

Fig. 1: Class E amplifier scheme.

Assuming the active device as an ideal switch (i.e., without losses), and the device output capacitance C_{ds} included in C_1, the output network is optimized to fulfil ideal Class E statements: i.e., a purely sine wave current waveform across the load R_L [6, 7] and zero voltage and zero derivative voltage switching conditions (respectively ZVS and ZVDS) across the active device [1, 2]. It can be noted that when the switch is on, the drain voltage is zero; and conversely, when the switch is off, the current flowing in the active device is zero. As a consequence, simultaneous nonzero voltage and current values are avoided, eliminating device power losses in the two states.

The capacitor C_1 (including the device C_{ds} output capacitor, possibly externally increased) is used to minimize switching losses during the on/off transition, i.e., to assure that the drain voltage starts increasing from zero just after the switch current is zeroed. The L_2 and C_2 element values are selected to minimise switching losses during the off/on transition, i.e., to assure that the drain voltage nulls just before the switch current increases, and to filter out the fundamental frequency component only.

The resulting ideal current and voltage waveforms are reported in Fig. 2.

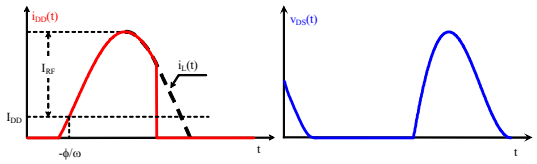

Fig. 2: Class E ideal current and voltage waveforms.

Assuming an operating pulsation ω, a quiescent supplied current I_{DC} and a purely sine wave current in the load R_L, i.e.

$$I_{tot}(t) = I_{DC} + I_{RF} \cdot \sin(\omega t) \tag{1}$$

Applying Kirchhoff and physical (energy conservation between C_1 and $C_S L_S$) laws, useful design relationships can be inferred, as reported in the following.

For the conduction angle α (refer to Fig. 2)

$$\tan(\alpha) = -2/\pi \tag{2}$$

The maximum peak current and voltage values become respectively

$$I_{Pk} = I_{DC} \cdot \left[1 + 1/\sin(\alpha)\right] \tag{3}$$

$$V_{ds,\max} = V_{DC} \cdot \pi \cdot \{2\pi - 2\alpha\} \tag{4}$$

while the fundamental current becomes

$$I_{RF} = I_{DC}/\sin(\alpha) \tag{5}$$

Moreover, the bias point (I_{DC} and V_{DC}) are related through C_1 value

$$I_{DC} = V_{DC} \cdot \pi\omega C_1 \tag{6}$$

The optimum load resistance becomes

$$R_L = 2\left(V_{DC}/I_{DC}\right) \cdot \sin^2(\alpha) \tag{7}$$

Therefore assuring an output power

$$P_{out} = 1/2 \cdot I_{RF} \cdot R_L^2 \tag{8}$$

L_S and C_S have to be designed to assure a highest quality factor Q filter around ω, i.e.,

$$\omega = 1/\sqrt{L_S \cdot C_S} \tag{9}$$

while the residual inductor L become

$$X_L = \frac{\pi}{2} \cdot \frac{V_{DC}}{I_{DC}} \cdot \left[\cos^2(\alpha) - \sin^2(\alpha)\right] \tag{10}$$

By using eqns. (2) to (10) and by taking into account device physical constraints, i.e., maximum current (I_{max}) and voltage (breakdown) limit (V_{BR}), it is easily to infer design quantities. Moreover, from the previous equation is it possible to derive the maximum operating frequency for an ideal Class E amplifier, resulting in

$$f_{\max} = \frac{I_{\max}}{V_{BR}} \cdot \frac{1}{C_1} \cdot \frac{\arctan\left(\frac{2}{\pi}\right)}{\pi \cdot \left[1 + \sqrt{\frac{\pi^2}{4} + 1}\right]} \tag{11}$$

The above relations, inferred by a time domain analysis, can also be obtained using frequency domain approach, obtaining for the fundamental load seen by the device the following impedance value [7]:

$$Z_{E,1} = \frac{0.28 e^{j49^\circ}}{\omega C_1} // \frac{1}{\omega C_1} = \frac{0.35}{\omega C_1} e^{j36} \tag{12}$$

From the above equations, it can be stressed that the output power is usually a free variable, which defines through eqns (4) to (8) the output network elements and in particular the output capacitance C_1. Of course, the maximum output power levels are limited by device physical constraints (I_{max} and V_{BR}) through eqns. (3) and (4). Moreover, to fulfil design statements, the capacitance C_1 has to be higher than the intrinsic device output capacitance, which therefore fixes the maximum operating frequency through eqn. (11), resulting in the inherent limitation of classical Class E design for high frequency applications.

III. High Frequency Class E Design Criteria

The availability of closed form expressions, as reported in previous section, for the design of a very efficient and mainly non-linear amplifier, justify the attractiveness of Class E approach. However, eqn. (11) shows its practical limitation in frequency, since by exceeding this maximum value, the ideal class E conditions and wave shaping (ZVS and ZVDS) cannot be further satisfied.

Moreover, for micro and millimetre-wave range applications the available active devices usually do not act as ideal switches, due to their not negligible parasitic effects, which increase switching time transitions and behave as low pass filters, practically shorting the higher frequency drain voltage components and consequently not allowing the desired wave-shaping. Thus, to modify ideal Class E conditions and to infer other optimum design criteria for high frequency applications, the above mentioned limitations have to be taken into account, considering a limited number of harmonic loads that can be effectively controlled and whose effects are relevant. In fact, from a practical point of view, only the first few (let's say up to the third) voltage harmonic components can be considered while the higher components can be assumed as effectively shorted, therefore neglecting their effects. Assuming for the moment the ideal waveforms reported in Fig. 2, and taking into account the relationships inferred in previous section, the active device bias point has to be optimised by the following criteria [7]

$$I_{DD} = 0.3494 \cdot I_{\max} \tag{13}$$

$$V_{DD} = \min\left[\frac{1}{3.562} \cdot V_{BR}, \frac{0.0177 \cdot I_{\max}}{f \cdot C_{ds}}\right] \tag{14}$$

by which last equation accounts for the practical limitations on the minimum value of C_1 (represented by the intrinsic device capacitor C_{ds}) and prevents breakdown phenomena due to the voltage overshooting behaviour.

Applying a frequency domain analysis on the ideal waveforms reported in Fig. 2 [7], but truncating the voltage Fourier representation to the first terms, the waveform resulting is reported in Fig. 3.

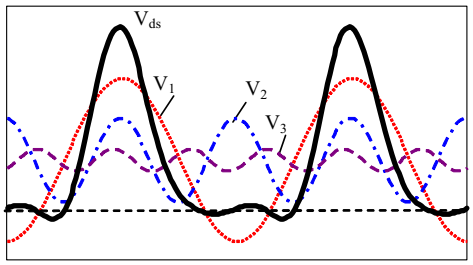

Fig. 3: Class E drain voltage waveform obtained truncating its Fourier representation up to the third harmonic component.

From this figure, two solutions can be adopted to prevent negative drain voltage values: Increasing the DC bias voltage V_{DD} with respect to the value expressed in eqn. (14), without violating the device physical limitations, or by modifying the fundamental load termination with respect to the value in eqn. (12). In the first case, increasing V_{DD} implies the increase of the dc power supplied P_{dc} and of the dissipated power in the active device (P_{diss}), thus decreasing the drain efficiency η with respect to the ideal case. Moreover, such solution could be unfeasible due to the increase in the peak voltage value, which could exceed breakdown limitations.

In the second case, assuming unaffected harmonic voltage components (i.e., V_2 and V_3) the optimisation implies finding the best V_{DD} and V_1 components in order to fulfil device constraints. This non-linear problem can be solved through numerical algorithms, resulting in an almost negligible increase of dc drain voltage (3%), but in a sustainable modification of V_1 and thus in the fundamental load impedance, which modulus has to be decreased by 13.5% while the phase should be slightly increased (less than 1%, which implies less than 5°). Moreover, the theoretical maximum efficiency decreases from 100% to 78%.

In the following section, two examples of Class E amplifiers designed according to high frequency criteria and based on GaAs PHEMT and on AlGaN/GaN devices will be presented.

IV. High Frequency Class E Design

In order to validate the Class E high frequency criteria, a first PA has been designed for X-Band application. In particular a 0.5 µm GaAs PHEMT device (1500 µm gate periphery) has been adopted, provided by Selex Sistemi Integrati (Italy). The device, which breakdown voltage and maximum current are 18V and 400mA respectively, has been characterised and modelled by a non-linear neural network model [8]. The design started computing the fundamental load impedance, according to eqn. (12), assuming an operating frequency of 9.6 GHz. The loads for the second, third and higher harmonics should behave as open circuits.

The capacitance C_1 in eqn. (12) is composed by the intrinsic device capacitance plus an additional external capacitance. Usually the latter is added in order to achieve a target output power, but this will decrease the frequency range for class-E operation. Therefore, for high frequency applications, this capacitance C_1 is reduced basically to the intrinsic output capacitance. Moreover, for sake of simplicity, the device output capacitance has been assumed linear. Actually, the non-linear output capacitance can be represented equivalently by a linear capacitance for Class-E design purposes [9]. The value of this output capacitance can be defined by small-signal extraction or by a load-line method (if a non-linear model is available). It is determined that the value of this capacitance is approximately 0.32 pF. The DC operating point is set close to pinch-off and has been tuned taking into account stability considerations and maximum allowable drain voltage, resulting in a gate voltage of -0.8 V and a drain voltage of 5 V.

The preliminary value of fundamental load, determined by (12) (9.5+j1.1 ohm), has been tuned to optimise the Class E behaviour, resulting in the final load (9.7+j13.4 = $16.5e^{j54°}$). Finally, the input matching network has been defined by determining the complex conjugate of the impedance seen at the gate terminal. Additional work was performed to keep the device and the amplifier stable over a broad frequency range, since it became conditionally stable over a range of frequencies around and including the operating frequency. Such stabilization was realized by using a shunt gate resistor. The resulting amplifier layout, realised in MMIC version by using stub elements is reported in Fig. 4.

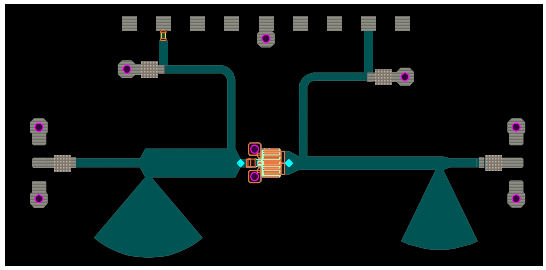
Fig. 4: 9.6 GHz GaAs Class-E Power Amplifier Layout.

The simulated time domain waveforms are depicted in Fig. 5, while the performances are shown in Fig. 6.

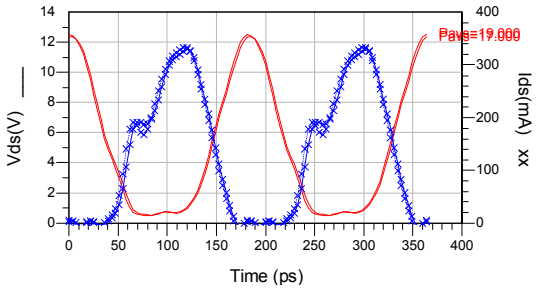

Fig. 5: Intrinsic drain voltage and current waveforms for the GaAs Class E design.

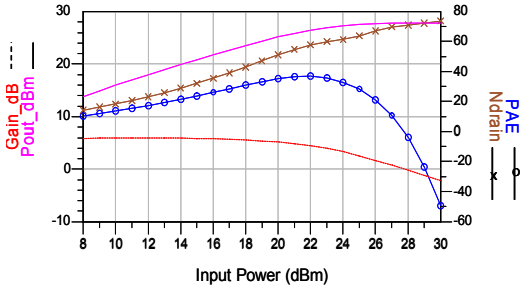

Fig. 6: 9.6 GHz GaAs Class-E PA performances.

A second Class E PA has been designed for C-Band application, by using an AlGaN/GaN HEMT with 1mm

gate periphery (10x100µm gate fingers) provided by Selex. Such device has a breakdown voltage of 70 V and maximum current of 400 mA and has been modelled by an Angelov model [10]. For this device, an output capacitance of 0.23 pF has been inferred, which has been assumed as C_1. The operating frequency was 2.4GHz, therefore higher than the maximum allowed by eqn. (11). In this case a hybrid approach has been adopted to design the Class E amplifier, resulting in the scheme reported in Fig. 7. The preliminary value of fundamental load, determined by (12) (53+j61 ohm), has been tuned to optimise the Class E behaviour according to the observation of previous section (obtaining 80+j54 ohm).

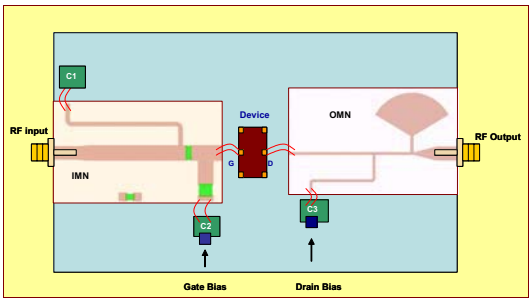

Fig. 7: 2.4 GHz GaN Class-E PA scheme.

For this amplifier, due to the high breakdown voltage characteristic of the GaN device, the gate voltage is fixed to -0.8 V while the drain voltage is 20 V. In this case the stabilization was realized by using a series and shunt gate resistor. The resulting voltage and current waveforms and amplifier performances are reported in Fig. 8 and Fig. 9 respectively.

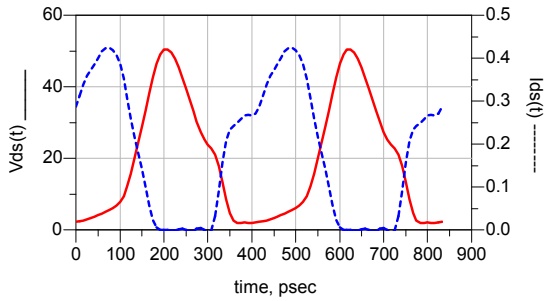

Fig. 8: Intrinsic drain voltage and current waveforms for the GaN Class E PA design.

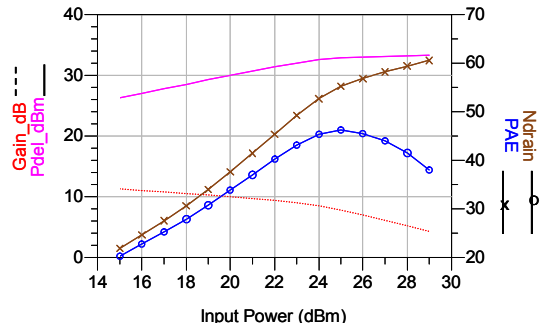

Fig. 9: 2.4 GHz GaN Class-E performances.

From time domain waveforms can be observed that the Class-E ZVS condition [1,6] is not fulfilled, which can be expected since a linear output capacitance was assumed. The phase of the fundamental load should be higher than 49 degrees in non-linear case [11]. On the other hand, the peak current and voltage are lower than the values expected in a linear ideal case. This comes from the fact that both amplifiers are working in frequency range slightly higher than the maximum optimal Class-E frequency [eqn. (11)], which is feasible but with suboptimal operation, which implies effects like the one just indicated.

V. Conclusions

In this paper the classical design criteria for Class E amplifier have been reviewed and extend for high frequency applications. In particular, starting from classical Class-E formulas, practical limitations arising in high frequency applications, due to a non ideal switching behaviour and device output capacitive shunting behaviour, have been discussed. High frequency design criteria have been presented and validated through the design of X-Band GaAs based and C-Band GaN based Class E amplifiers.

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