# GaN H-FET development at QinetiQ

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*Abstract* — **The AlGaN/GaN HFET project at QinetiQ has the capability to grow high quality layers using MOVPE, fabricate HFETs with 0.8 and 0.25µm gate length and fabricate amplifiers. Here we present recent work on topics as diverse as X-ray determination of aluminium concentration, 0.25Ohm.mm Ohmic contacts, measurement of saturated velocity, current slump and a 57W hybrid amplifier.**

## I. Introduction

QinetiQ has been active in GaN HFET development since 1998, fabricating its first transistors in 1999. The project is vertically integrated with a full capability in place including epitaxy with its material and electrical characterization, device processing, circuit fabrication and modeling.

This article will give an overview of the capability and highlight some of the most recent developments from QinetiQ and its collaborators.

## II. Epitaxy

### *A. Epitaxial Process*

The epitaxial growth is carried out in a Thomas Swan close-coupled “showerhead” MOVPE reactor. This vertical geometry platform is used to grow on wafers from 2inch up to 4inch diameter with excellent cross-wafer uniformity. A custom spectral reflectance system has been implemented which gives real-time feedback on epi quality, and has been used to refine the process and establish good run to run reproducibility.

The standard structure is 30nm undoped $Al_xGa_{1-x}N$ (x=0.28), 1.2µm GaN (undoped) on either sapphire or SiC substrates with the appropriate nucleation layer. Here we report results for the layers grown on SI 4H SiC.

### *B. Measurement of Aluminium Content*

A key issue for the control of the epitaxy is the Al concentration in the AlGaN layer. The standard technique for measuring composition in ternary layers is x-ray diffraction. However, for hexagonal GaN this normally requires up to 6 measurements to be made in order to allow the effects of strain and composition to be separated. The low thickness of the barrier layer (typically 20-30nm) exacerbates this as data collection times are extended. A further consideration in the GaN/AlGaN system is the large variation in literature values of the elastic constants, which places an ultimate limit on the accuracy with which composition may be determined. We have recently demonstrated a new technique which allows the AlGaN composition to be accurately determined from a single X-ray measurement and reduces the errors associated with the uncertainty in elastic constants[1]. This method uses the fact that changing the composition of an alloy is expected to change the crystal plane spacing in all three dimensions, i.e. it introduces a hydrostatic strain. In contrast, biaxial strain in the plane of the epi-layer gives a strain of opposite sign in the growth direction. There will therefore, be directions in the crystal in which the atomic spacing is not sensitive to biaxial strain, only hydrostatic strain. Thus, by measuring a plane spacing in such a direction, it is possible to estimate the alloy composition in a partially relaxed crystal using a single measurement. Additionally, since the effect of biaxial strain is minimized, the sensitivity of the measurement to the chosen value of elastic constants is also minimized. Hence, using the (20.5) reflection allows the straightforward determination of composition with confidence and accuracy.

## III. Processing

### *A. Standard Processes*

The process employed is a standard mesa isolated HFET process. The mesa is etched using $SiCl_4$ RIE, and the Ohmics use a Ti/Al/Pt/Au recipe. The gate is either a 0.6-0.8µm gate for S-band operation, or a 0.25µm T gate for X-band. Passivation is carried out using a PECVD silicon nitride layer. The process is completed with a plated gold metal airbridge.

### *B. Ohmic Optimisation*

The Ohmic contact has been the subject of considerable recent development. A typical value of contact resistance of 1-2Ohm.mm was obtained prior to optimization. This high value produces a very significant fall in transconductance and $I_{dss0}$ and is essentially unacceptable, especially if there is a variation from wafer to wafer (the low field source-drain resistance of the

entire channel is normally only about 1.5-2Ohms). The contact resistance has now been improved to below 0.5Ohm.mm which is satisfactory for the targeted applications. Currently we use Ti/Al/Pt/Au of nominal thicknesses 10/120/25/50nm alloyed at 795°C for 30secs. Interestingly, this metallization gives consistently higher values of $R_c$, by around 0.25 Ohm.mm, for our standard epitaxial structure on sapphire as compared with our standard epitaxy on SiC substrates. The control of several parameters was found to be important in the contact resistance improvement. The process improvements involved a combination of $SiCl_4$ RIE pre-etch optimization, modification of the rapid thermal anneal temperature profile and ambient as well as changes to the thickness of the metal layers and the metal ratios. Ensuring that alloying occurred immediately following evaporation of the metal layers was also important since reaction of Al and Pt occurs even at room temperature. An example of a recent map of contact resistance is seen in Figure 1 where a contact resistance of 0.18±0.06Ohm.mm was achieved to a layer of 512±20Ohm/sq.

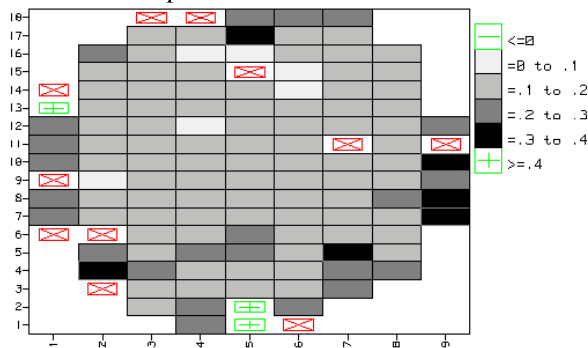


Figure 1. Map of contact resistance in units of Ohm.mm.

Equally as important as the contact resistance is the edge morphology of the contact. Like most Al based Ohmic recipes, the final surface is rough after anneal, but a reasonable compromise has been obtained with quite acceptable edge definition as can be seen in Figure 2.

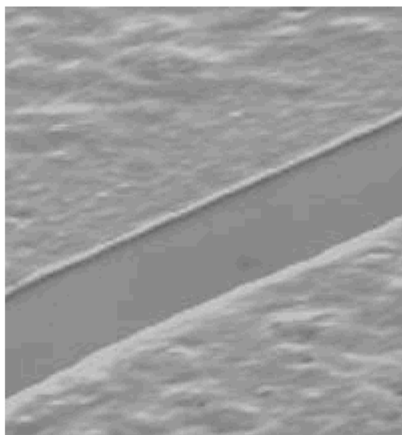

Figure 2. SEM of contact morphology showing a 5µm gap.

## IV. Device and Circuit Results

### *A. Saturated Velocity*

A key parameter in determining the ultimate frequency performance of the device is the saturated velocity. This has been the subject of considerable discussion and work in the literature targeted at understanding the apparent discrepancy between the values predicted by Monte-Carlo simulation (~$2.5\times10^7$cm/s) and those obtained experimentally from the device characteristics (always around $1\times10^7$cm/s). Working with De Montfort University, we have examined carefully the equivalent circuit model required to extract the saturated velocity from the S-parameter measurements[2]. Three different effects were included in the analysis: a) the effective lengthening of the gate by the geometrical fringing fields at the edges of the gate, b) the quasi-static charge model for the terminal capacitances, and c) the extension of the drain depletion region under high applied bias. Figure 3 shows how the saturated velocity varies with gate and drain bias for a 0.29µm gate length transistor. A peak saturated velocity of only $1.2\times10^7$cm/s was obtained. The saturated velocity was relatively independent of drain voltage (despite the fact that the junction temperature rise was up to 140°C), but most interestingly fell rapidly as the gate voltage was increased towards open channel. These results are very consistent with the hot-phonon model for charge scattering[3]. This states that the exceptionally high carrier concentration in the 2DEG channel combined with a phonon lifetime of around a picosecond results in an accumulation of hot phonons which increases the scattering rate[4]. The implication is that the ultimate speed of GaN power HFETs may not be quite as high as was initially hoped.

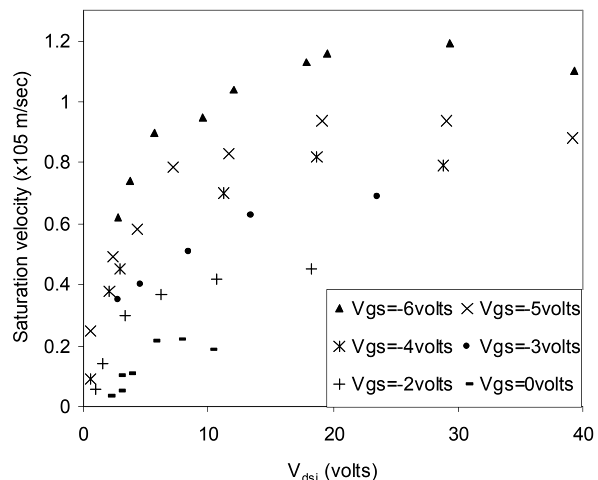


Figure 3. Saturated velocity of 2×50µm HFET

### *B. S-Band Power Devices Characterisation*

S-band power devices have been fabricated with a 0.8µm gate length. The wafer had a contact resistance of 2±0.38Ohm.mm, leading to $I_{dss0}$ of 700mA/mm, and $g_m$ of 120mS/mm. These devices show very little gate lag,

and start to show significant drain lag only for $V_d$>30V. The RF power performance has been assessed in collaboration with Cardiff University using their time domain RF measurement facility, they found a peak power density of 4.3W/mm in class A and 5.5W/mm in class F[5, 6].

Operating the device in a class A mode, Figure 4 shows how the knee-walkout associated with current slump can be seen in the pulse-IV measurement when compared to the open channel characteristic.

Pulse-IV provides a simple method of characterizing most devices since it allows the extent of the load-line to be mapped without RF measurement. The RF load-line has been obtained from time domain RF measurements at 840MHz for a range of class A bias points as shown in Figure 5. Load-pull is used to optimize the output power in each case. It can be seen that there is good agreement with the pulse-IV measurement for a gate bias of +2V, corresponding to a typical maximum forward RF gate voltage swing in saturation. Interestingly, the agreement is not as good for higher order modes such as class B and F.

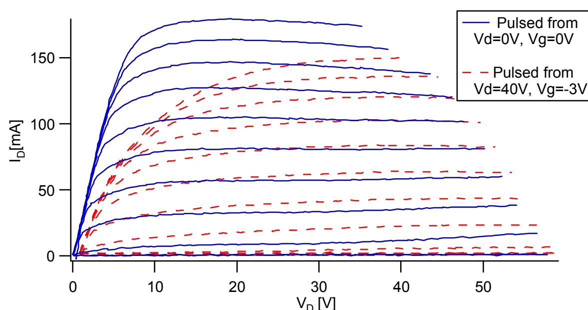


Figure 4. Pulse IV of 200×0.8µm device with Vgs= -8 to +2V step +1V. 1µs/1ms pulses.

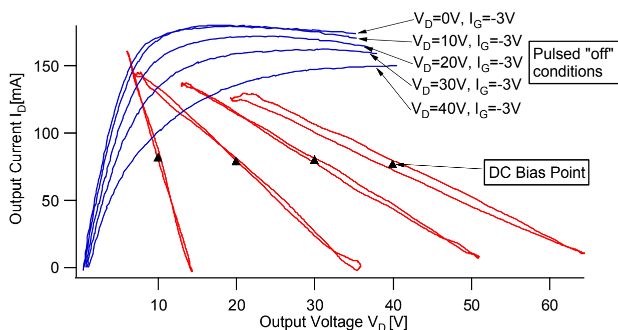


Figure 5. Comparing pulse-IV for Vgs=+2V, measured at the indicated operating points with RF load-line.

### *C. S-Band Hybrid Power Amplifier*

S-band power bars with 0.8µm gate length and power cell dimension of 4×500µm with 50µm finger pitch are included on the wafer. They have been used to assemble a hybrid power amplifier using a total of 24mm of transistor width. This amplifier gave a maximum output power of 57.5W with 3dB compression, 32% power added efficiency as shown in Figure 6.

## V. Conclusion

An overview of some of the recent developments undertaken at QinetiQ has been presented. This includes progress in epitaxy, device processing, device physics and power amplifiers.

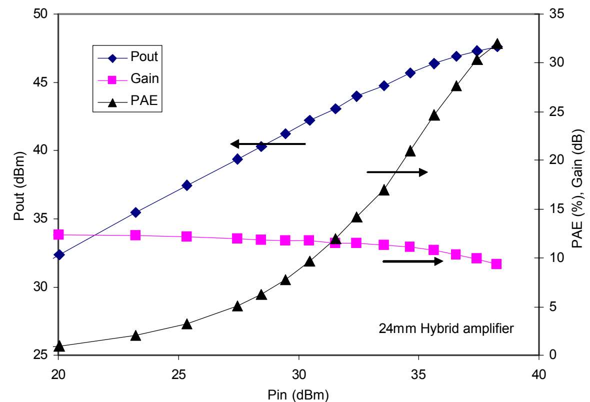


Figure 6. RF performance of a 24mm wide hybrid amplifier operating at 2.7GHz, 1ms pulse length, 10% duty, $V_d$=30V.

## Acknowledgement


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## References


[1] D. J. Wallis, A. M. Keir, R. S. Balmer, D. E. J. Soley, and T. Martin, "Composition measurement in strained AlGaN/GaN epitaxial layers using X-ray diffraction," *Applied Physics Letters*, vol. 85, pp. 6359-6361, 2004.

[2] C. H. Oxley and M. J. Uren, "Measurements of unity gain cut-off frequency and saturation velocity of a GaN HEMT transistor," *IEEE Trans. Electron Devices*, vol. 52, pp. 165-169, 2005.

[3] B. K. Ridley, W. J. Schaff, and L. F. Eastman, "Hot-phonon-induced velocity saturation in GaN," *Journal of Applied Physics*, vol. 96, pp. 1499-1502, 2004.

[4] A. Matulionis, J. Liberis, L. F. Eastman, and Y.-J. Sun, "Drift velocity saturation and hot-phonon disintegration in AlGaN/AlN/GaN channels," in *Compound Semiconductor Devices and Integrated Circuits (WOCSDICE 2005)*, A. Porch, R. Perks, and V. Morgan, Eds. Cardiff, 2005, p. 71.

[5] P. McGovern, P. J. Tasker, J. Powell, K. P. Hilton, R. S. Balmer, T. Martin, and M. J. Uren, "Experimental Investigation of DC-RF Dispersion in AlGaN/GaN HFET's Using Pulsed I-V and Time-Domain Waveform Measurements," in *Proceedings of CS-MANTECH, New Orleans, LA, April 2005*, 2005.

[6] P. McGovern, P. J. Tasker, J. Powell, K. P. Hilton, R. S. Balmer, T. Martin, and M. J. Uren, "Experimental Investigation of DC-RF Dispersion in AlGaN/GaN HFET's Using Pulsed I-V and Time-Domain Waveform Measurements," in *Proceedings of International Microwave Symposium, Long Beach, CA, June 2005*, 2005.