Low-Power GaAs Multiplexer and Demultiplexer

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Abstract

For the implementation of high-complexity circuits operating at high speed, low-power circuits are essential in order to meet chip level and systems level power dissipation requirements. This paper presents the designs of a multiplexer and a demultiplexer. The circuits are implemented by using two-phase dynamic FET logic (TDFL). Two chips were designed. Each chip comprises a small system integrating normal TDFL logic, pass gates and domino logic as well as clock drivers. Measurements show that the multiplexer operates at $300MHz$ and the demultiplexer operates at $550MHz$

Introduction

For the implementation of high-complexity circuits operating at high speed, low-power circuits are essential in order to meet chip level and systems level power dissipation requirements.

High speed can be obtained by using source-coupled FET logic (SCFL) or direct-coupled FET logic (DCFL) at the expense of a relatively high power consumption. These logic families can be used for high speed off-chip communications. Often, however, on-chip processing can be performed at a lower speed. For this purpose two-phase dynamic FET logic (TDFL) [1] offers superior speed/power performance.

In this paper, a low-power multiplexer and demultiplexer are presented. The circuits are implemented by using TDFL.

TDFL functionality

The operation of TDFL follows a precharge/evaluate scheme. The two-input NOR gate shown in Figure 1 precharges when *phi 1* is high, and evaluates when *phi 2* is high. TDFL is a sequential logic family, which means that gates precharging on *phi 1* should be followed by gates precharging on *phi 2*.

The depletion-mode MESFETs (DFETs) have $V_t = -0.8V$ and the enhancement-mode MESFETs (EFETs) have $V_t = 0.2V$. In order to turn off the DFETs, the low level of the clock signal is chosen to be $-1V$. The high level is $0.5V$ where the DFETs are turned on, and the gate-source Schottky conduction is still negligible.

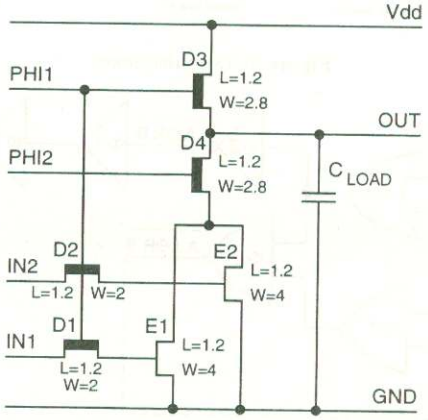

Figure 1: TDFL two-input NOR gate

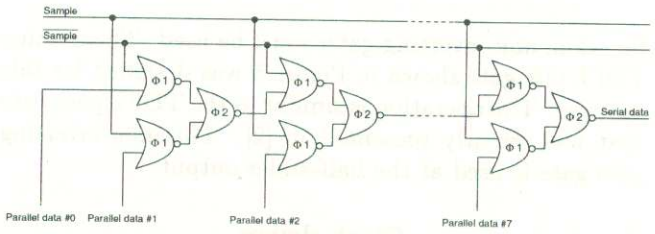

Figure 2: Multiplexer

During precharge the output is precharged to $V_{dd} = 1.2V$. If one or both of the inputs are high, the output will be discharged to $0V$ during the evaluate phase. If both inputs are low, the output is discharged to approximately $0.5V$ by the EFET gate-source Schottky diode of the following stage.

TDFL circuits

An 8 to 1 multiplexer and a 1 to 8 demultiplexer was designed using TDFL. The multiplexer is implemented as a shift register with parallel load as shown in Figure 2. The gates in the multiplexer are two-input TDFL NOR gates.

The demultiplexer is shown in Figure 3. It consists of a shift register implemented by TDFL inverters and enable flip-flops implemented by using two-input NOR gates.

A systolic counter was designed for the generation of byte synchronisation signals for the multiplexer and demultiplexer. The counter was built from half adders, as shown in Figure 4. In order to implement the XOR

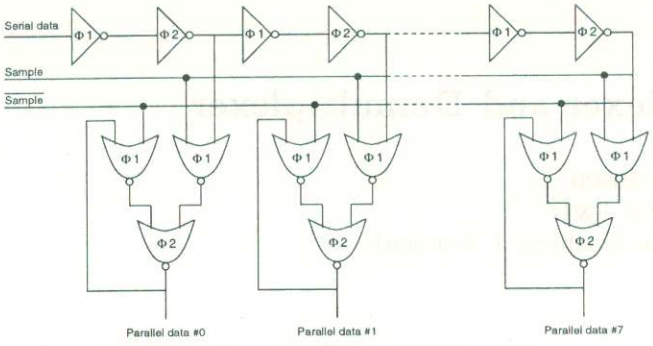

Figure 3: Demultiplexer

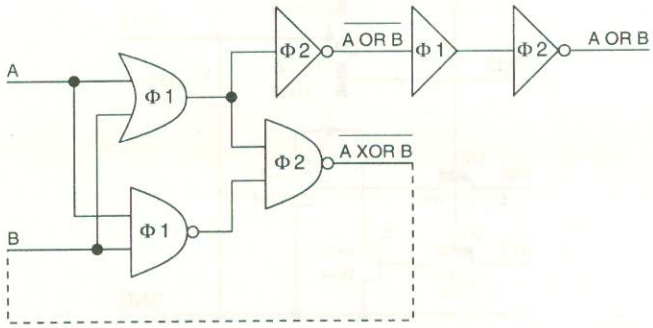

Figure 4: Half-adder

function, non-inverting gates must be used. The domino TDFL OR gate shown in Figure 5 was designed for this purpose. The operation is similar to the TDFL pass gate that was resently presented in [2]. This non-inverting pass gate is used at the half-adder output.

Clock driver

The clock signals are generated on-chip using a novel TDFL clock driver. To the knowledge of the author there have been no reported attempts to implement on-chip TDFL clock drivers. The clock driver architecture is shown in Figure 6.

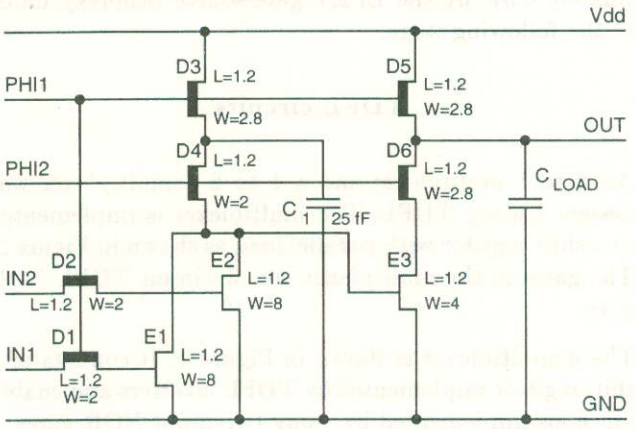

Figure 5: TDFL two-input domino or gate

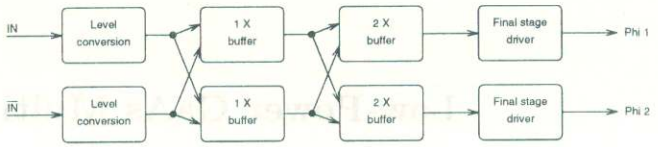

Figure 6: Clock driver

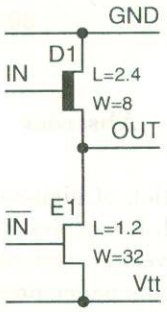

Figure 7: Clock driver buffer (size 1 X)

Initially the differential signal from the pad receiver is level shifted from DCFL levels with reference to GND to DCFL levels with reference to Vtt.

The signals are amplified in a two-stage buffer chain. The buffer is shown in Figure 7. It is a DCFL inverter which has improved pull-up speed by applying complimentary data at the DFET gate. This furthermore has the advantage that any unbalance in the differential input data will be diminished.

The final-stage of the clock driver is shown in Figure 8. The operation can be seen as an enhanced super buffer or a reduced ultra buffer [3].

The final stage clock driver is driven by a DCFL-type signal with reference to $V_{tt} = -1V$. When the input is high, both node A and the output are pulled low.

When the input goes low, D1 will pull node A high, and the output will be pulled high by E4. When the output voltage exceeds the threshold voltage of the EFETs, E2 will start pulling down node A. D1 and E2 are sized so that the high level of the output is $0.5V$.

Thus the required voltage swing of $[-1V; 0.5V]$ is gener-

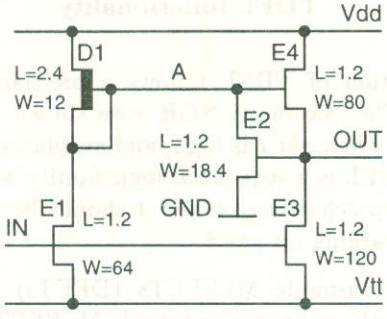

Figure 8: Final stage clock driver

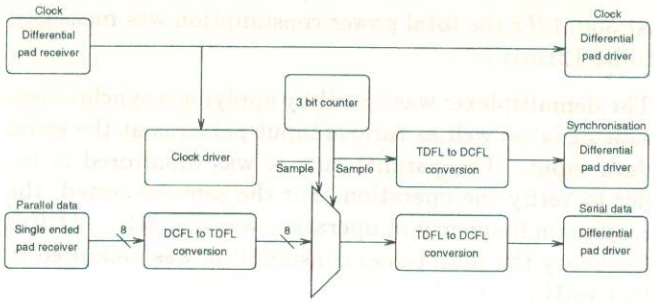

Figure 9: Multiplexer chip

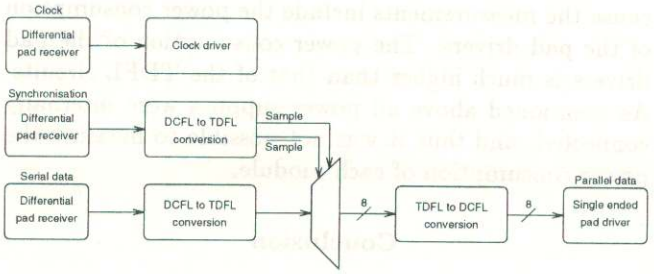

Figure 10: Demultiplexer chip

ated. Furthermore, it can be seen that the E3/E4 stage has only dynamic power consumption. This results in a considerably lower power consumption compared with pure DCFL or super buffer clock drivers.

Implementation

The circuits were implemented on two separate chips. One chip contains the multiplexer and systolic counter, whereas the other contains the demultiplexer. The clock driver is included on both chips.

The architectures of the two chips are shown in Figure 9 and Figure 10. Conversion circuits from DCFL to TDFL levels and back are included in order to interface the TDFL circuits to pad receivers and drivers.

¡The chips were layed out using MAGIC. In order to minimize noise the power supply to all modules were connected on-chip.

Operation was verified in HSPICE. Simulations were performed in the temperature range from -55^0C to 125^0C. Despite optimisations on sizing and circuit topology, successful operation could not be simulated above 75^0C. A possible explanation for this is that the leakage currents increases at higher temperatures making the lower frequency of operation meet the upper.

The operation of TDFL is highly dependent on the parasitic capacitance at the output. For that reason the parasitic capacitances of the TDFL outputs were controlled to be at least $30fF$ with typical values of $35fF$.

Table 1: Power consumption simulated at $500MHz$

Module name	Power	Gates	Power/gate
Multiplexer	$0.5mW$	21	$24\mu W$
Demultiplexer	$0.9mW$	40	$23\mu W$
Counter	$0.5mW$	19	$26\mu W$
Clock driver	$6mW$	-	-

Fabrication was carried out in the TCS SAGA 0.8μ process through CMP in France. Chip photographs are shown in Figure 11 and Figure 12. The die size is $2.5mm$ by $2.6mm$.

Comparison

An overview of the power consumption of the modules is shown in Table 1. As can be seen, the TDFL circuits have an extremely low power consumption.

The low power consumption of TDFL is obtained because the gates have only dynamic power consumption. During each clock cycle, the output is precharged to V_{dd}. For most of the gates in the design, the parasitic capacitance at the output is approximately 35 fF. Assuming that the capacitor gets totally discharged during all clock cycles, the energy used in each clock cycle becomes $35fF \times 1.2V^2 = 50fJ$. At $500MHz$, this corresponds to $50fF \times 500MHz = 25\mu W$, which is in close agreement with the simulation results shown in Table 1.

In order to compare with a standard 0.8μ CMOS inverter constructed from minimum-size transistors, we assume gate and drain capacitances of $5fF$ and $30fF$ routing capacitance. The total capacitance affected each time the inverter switches is thus $50fF$. The energy dissipated each time the inverter switches is given by $0.5 \times 50fF \times 5V^2 = 625fJ$.

As can be seen, the power consumption of TDFL is an order of magnitude lower than that of standard CMOS. This advantage becomes even larger if the high functionality of TDFL is taken into account.

Results

The chips were packaged in a 28 pin LDCC package. All testing was performed on packaged chips at room temperature.

Various patterns were applied at the parallel input of the multiplexer chip. The serial output and byte synchronisation signal were monitored in order to verify the functionality. For the samples tested, the maximum frequency of operation was 300 MHz. An example of the measurements is shown in Figure 13.

Above $300MHz$ both the data signal and the byte synchronisation signal disappeared, indicating that the operation is limited by the counter.

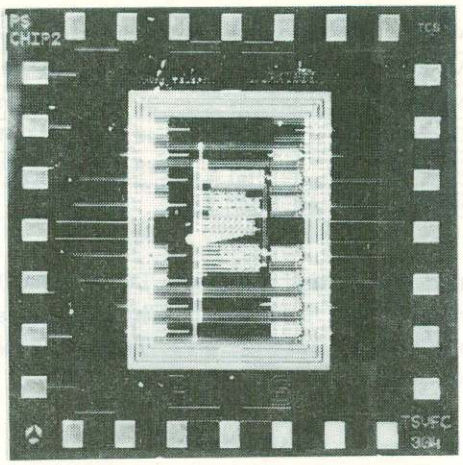

Figure 11: Chip photo of multiplexer chip

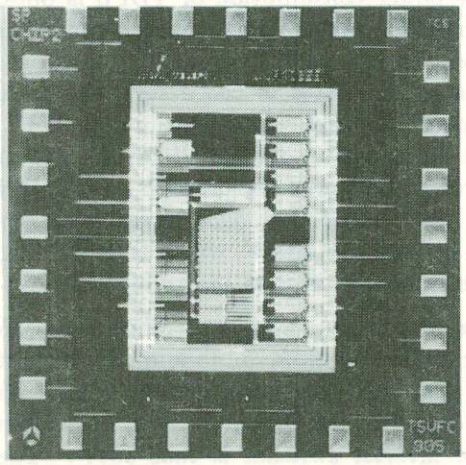

Figure 12: Chip photo of demultiplexer chip

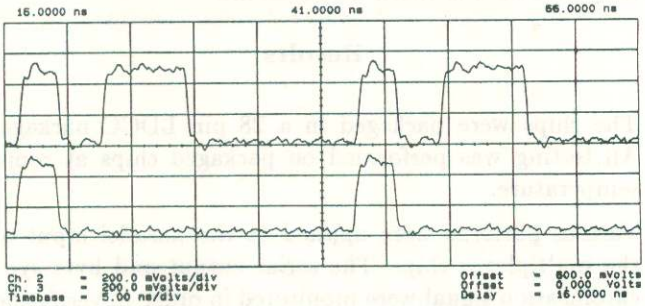

Figure 13: Serial output (top) and byte synchronisation (bottom) signals of multiplexer chip. The parallel input is "1011000"

At $300MHz$ the total power consumption was measured to be $121mW$.

The demultiplexer was tested by applying a synchronisation signal as well as various input patterns at the serial data input. The parallel output was monitored in order to verify the operation. For the samples tested, the maximum frequency of operation was 550 MHz. At this frequency the total power consumption was measured to be $64mW$.

It is difficult to compare the measured power consumption with the simulated values shown in Table 1 because the measurements include the power consumption of the pad drivers. The power consumption of the pad drivers is much higher than that of the TDFL circuits. As mentioned above all power supplies were internally connected, and thus it was not possible to measure the power consumption of each module.

Conclusion

The design of a multiplexer and a demultiplexer was presented. Low-power operation was obtained by using TDFL. The circuits were implemented on two chips. Each chip comprises a small system integrating normal TDFL logic, pass gates and domino logic as well as clock drivers.

The chips were tested and found to work. The maximum frequency of operation of the multiplexer was 300 MHz, and the maximum frequency of the demultiplexer was 550 MHz. All testing was performed on packaged chips.

The power consumption of the TDFL circuits was simulated to be approximately $25\mu W$ at $500MHz$, or $50fJ$ per clock cycle. This is an order of magnitude lower than that of standard CMOS.

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References

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[2] Peter S. Lassen. *High-Speed GaAs Digital Integrated Circuits for Optical Communication Systems.* PhD thesis, Technical University of Denmark, May 1993.

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