A GaAs Power Chip Set for 3 V Cellular Communications

Eric PUECHBERTY, Denis MASLIAH*, Etienne DELHAYE, Amparo HERRERA+

LEP/PHILIPS MICROWAVE LIMEIL
BP 15 - 22 avenue Descartes, 94453 Limeil Brévannes Cedex, France

* WAVECOM, 39 rue du Gouverneur Général Eboué, 92130 Issy les Moulineaux, France
+ UNIVERSITY OF CANTABRIA, Avenudas de los Castros, 39005 Santander, Spain

Abstract

This paper presents a chip set operating at 3 V supply voltage for cellular communications at L-band. A high efficiency power amplifier with a high packing density is reported. It makes use of high power-added-efficiency of MESFET devices in saturated class AB, and harmonic enhancement for the matching circuits. This three stage MMIC amplifier delivers 27 dBm output power with 35 % of power added efficiency with 0 dBm input power. A power switch is also described which achieves a typical insertion loss in the (0.8 dB, 1.0 dB) range and performs 20 dB isolation between the Rx (Receive) and Tx (Transmit) chains. PML also proposes a power MESFET that achieves 33 dBm output power with 55 % drain efficiency and 6 dB associated gain at 1800 MHz.

Introduction

RF integrated circuits for cellular communications will constitute a considerable market for the semiconductor industry in the 1995-2000 period, where GaAs technology will play an important role. Indeed, it is now widely recognized that the GaAs MESFET technology is particularly well suited for the implementation of the Tx power stages, where high power efficiency amplification is required at L-band; The trend towards weight and volume reduction in cellular communication handsets imposes power supply voltages to be reduced down to 3-4 V (3 times 1.1 V battery elements) for the next generation of terminals. This does not only hold for cordless systems but also for cellular mobile radiocommunication standards such as GSM (Global System for Mobile), DCS (Digital Cellular System) and PHP (Personal Handy Phone), even if this move will impose a modification of the GSM base station network.

The amplifier described below meets the requirements for the Digital European Cordless Telephone (DECT) commercial market and can be used either as a driver amplifier for Class I DCS or as Tx amplifier in Class II DCS handsets. The switch conforms to the DECT specifications and the power MESFET offers an optimal solution for Class I DCS.

Circuits fabrication

These power MMIC's have been fabricated using PML's 0.7 µm MESFET ERO7AD process. This process uses 3" LEC wafers, gate recessing, Si^+ implantation, boron isolation, contact photolithography, dry etching and enhanced lift-off techniques. Enhancement mode transistors (E-FET) and depletion mode transistors (D-FET) are available in this process, which both have a typical F_T of 17 GHz. The D-FET which is mostly dedicated to power applications, has a threshold voltage of - 2.0 V and the typical available power at 3V bias supply is 100 mW/mm. The E-FET threshold voltage is V_t = 0.175 mV.The substrate thickness is 200 µm and this low cost process does not use airbridges nor backvias.

Power Amplifier

1. Circuit Design

The power amplifier is designed to reach an output power over 27 dBm and a total efficiency higher than 30 % both in the DECT band (1880-1900 MHz) and DCS band (1710-1785 MHz) under 3.3 V supply voltage. The input power is set to 0 dBm.

In order to achieve high efficiency at a given DC current level, the load line has to be positioned well below the knee voltage in the IV characteristics, which imposes the use of high periphery D-FETs. At the same time, the load line of the transistor must be near the load line that gives the maximum gain, and the MESFET should be biased near pinch-off to minimize overlapping of the current and voltage waveforms [1].

Thus it comes that the transistor for power amplification and high efficiency must be biased in saturated class AB [2].

To achieve 27 dBm of output power, a three stage architecture was implemented. The photograph of the IC is shown in Fig. 1, the size of the chip is 2.3 mm².

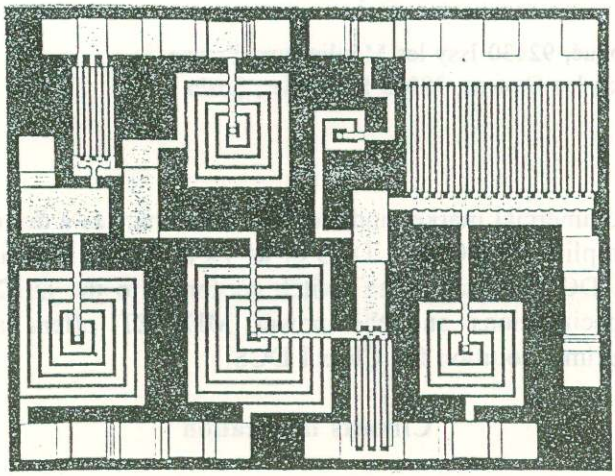

Fig. 1 Photograph of the 27 dBm power amplifier MMIC

The size of the MESFETs is fixed to ensure power output capability, as well as saturation. Feedback circuits are used on the first and second stage devices to ensure low frequency stability [3].

The linear gain of the three stages is 11 dB, 10 dB and 9 dB respectively. The required impedances for each of the three stages of amplification were extracted from load pull measurements. At this stage, the design effort consists in the synthesis of the interstage networks. A proper harmonic termination is responsible for the current and voltage waveforms and therefore directly influences the total efficiency and output power. We extended the Real Frequency Technique (RFT) [4] to look for the closest realizable solution to this problem. The advantage of the RFT is to include the harmonics in the calculation of the load impedance (short-circuit at the second harmonic and high impedance at the third harmonic). All biasing and matching networks are on chip except for the last stage because the DC current is too high and the Quality factor (Q) of integrated passive elements is too low. So we used a quaterwave length transmission line to bias the third stage.

2. *Measurements*

Extensive measurements of this power amplifier in both DECT and DCS band are reported below. In DCS (DECT) band, the output power measured is 27 dBm (26 dBm) for an input power of 0 dBm and a voltage supply of 3.3.V (3.0 V) ; the associated power efficiency is over 35 % (Figs 2 and 3).

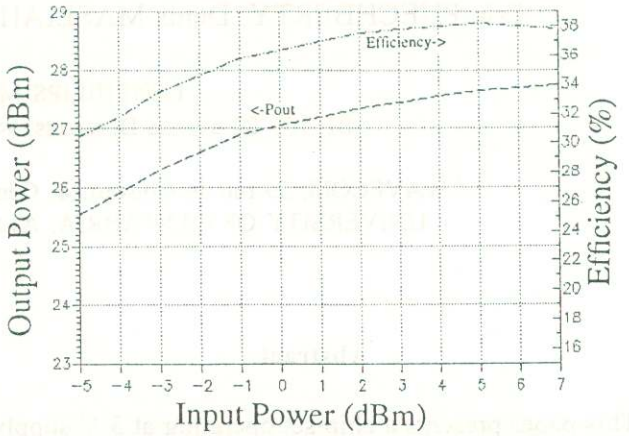

Fig. 2 Typical power transfer curves in DCS band. F = 1.75 GHz at 3.3 V

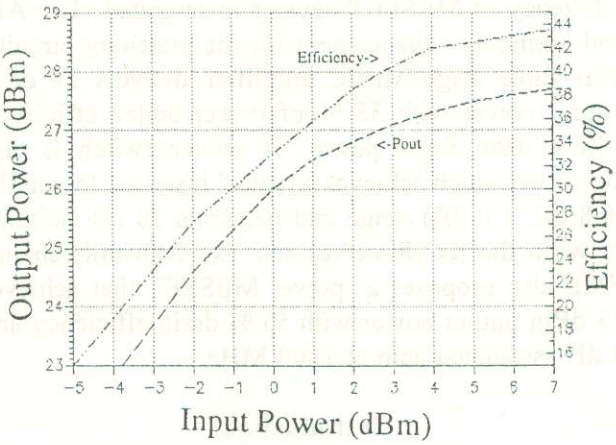

Fig. 3 Typical power transfer curves in DECT band. F = 1.9 GHz at 3.0 V.

The typical gate bias is - 1.2 V and the total gate current is lower than 300 µA for an input power pushed up to 5 dBm. This very low DC power consumption is a very important result from a system point of view for the generation of the negative power supply. Furthermore, the gain of the amplifier can be controlled and a dynamic range of 50 dB is obtained by applying gate voltages between -1.2 V and - 2.5 V.

A gain dynamic range of 55 dB is also obtained by the control of drain supply voltage (0 ; 3.3 V) ; with this configuration, the AM/AM conversion measured is lower than 2 %.

In the DCS standard, we measured the floor noise generated in the Rx band (1805-1880 MHz), an excellent performance of - 167 dBc/Hz or - 140 dBm/Hz was obtained.

The output - 1 dB compression point of this high efficiency power amplifier is 21.5 dBm and the second and third harmonic have a level lower than - 40 dBc for an input power of + 13 dBm.

A high power switch

A high power switch operating at low supply voltage that meets the DECT system requirements is presented. It makes use of the MESFET's high speed and RF power capabilities. A photograph of the chip is presented on Fig. 4, the total gate width is 16.2 mm and the size of the device is kept below 1 mm² (730 x 1 200 µm).

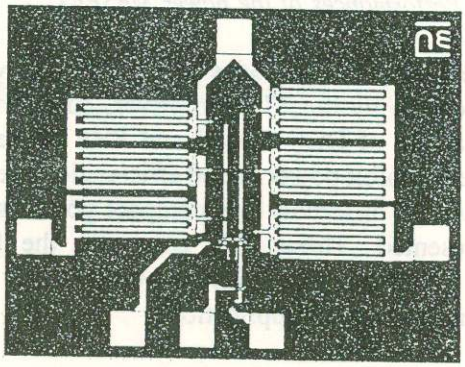

Fig. 4 Photograph of the power switch

This is a reflection type switch designed with D-FET transistors (Fig. 5). The gate width of the transmission (Tx) branch is optimized to obtain losses lower than 1 dB and to meet the saturated output power of 27 dBm [5]. The influences of the FET sizes are as follows :

- Insertion losses get lower as gate widths increase, but are hampered by leakage through the drain-source capacitance of the OFF device ;
- Good isolation requires limited gate width .

A compromise on these two specifications must therefore be achieved through proper sizing of the devices.

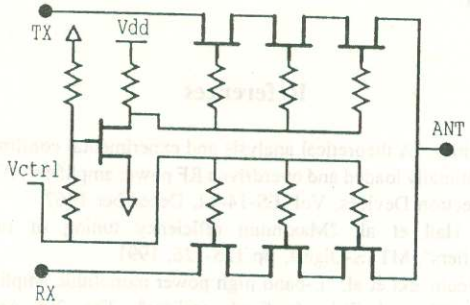

Fig. 5 Schematic of the power switch

When the Tx channel is ON, the full voltage swing is directly applied to the Rx channel FET and exceeds the maximum source-drain breakdown voltage of one single FET. Three FETs in series are therefore used to share the voltage on each device.

A unique external control voltage source is needed for both Rx and Tx channel and a E-FET transistor is used to generate the complemented signal of the command. We chose a floating electrode configuration in order to take advantage of the diode in forward condition to bias the common point (ANT).

Time domain simulations have been run, the ON/OFF switching delay is lower than 25 nS (Fig. 6) ; this performance exceeds the requirement of 30 µs.

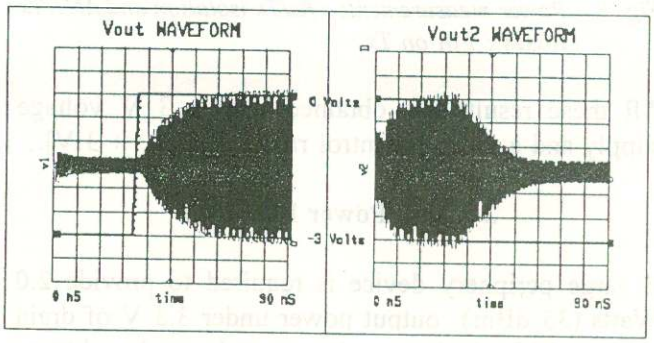

Fig. 6 Transient time switch response

Fig. 7 shows the measured performances of the Rx/Tx isolation and Rx/ANT losses when the input signal is on the antenna port. Typical results are : losses lower than 1 dB and isolation better than 17 dB for an input power (ANT) lower than 20 dBm.

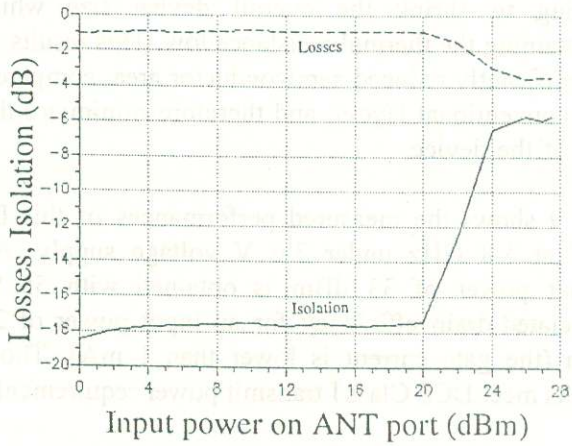

Fig. 7 Power measurements ; Rx/Tx isolation and Rx/ANT losses ; Pin on ANT

Fig. 8 shows the measured performances of the Rx/Tx isolation and ANT/Tx losses when the input signal is on Tx port. Typical results are losses lower than 1 dB, isolation better than 20 dB for an input power (Tx) lower than 28 dBm.

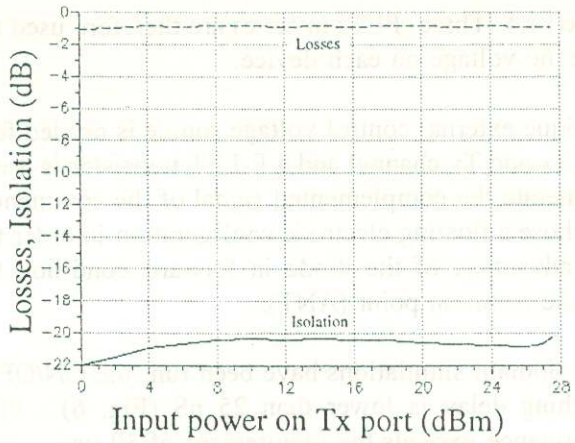

Fig. 8 Power measurements ; Rx/Tx isolation and ANT/Tx losses ; Pin on Tx

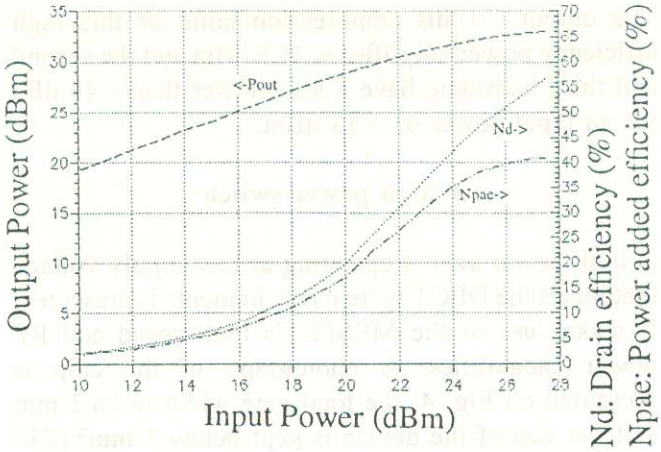

Fig. 9 Performances of the power MESFET

All these results are obtained with a 3 V voltage supply and a voltage control range of [- 2 ; + 3 V].

2 Watts Power MESFET

A large periphery device is required to provide 2.0 Watts (33 dBm) output power under 3.3 V of drain supply. This device needs not only to be able to provide the output power but must have a high efficiency to achieve low power consumption and low power dissipation.

The high efficiency behaviour is obtained by proper choice of the load line. We calculated that 24 mm of gate periphery was necessary to achieve 2.0 Watts with high efficiency. We optimize the gate to gate spacing to shrink the overall device size while maintaining the thermal resistance low. This results in a significantly reduced semiconductor area, compared to a conventional layout, and therefore minimizes the cost of the device.

Fig. 9 shows the measured performances of this D-FET at 1.8 GHz under 3.6 V voltage supply. An output power of 33 dBm is obtained with 55 % associated drain efficiency for an input power of 27 dBm (the gate current is lower than 1 mA). Those results meet DCS Class I transmit power requirements.

Conclusion

A complete power chip set operating at 3 V and suitable for all cellular and cordless communication standards in the 1700-1800 MHz band is presented. A 27 dBm compact power amplifier meets the Tx specifications of both DECT and DCS Class II standards, and can be used as a Tx driver in a DCS Class I architecture as well.

This chip set also includes a 33 dBm power FET which, driven by the 27 dBm driver, conforms to the specifications of DCS Class I and PHP hansets. Both amplifiers exhibit power added efficiencies in excess of 35 %. A low insertion loss compact power switch is also presented. These IC's constitute the basis of Philips Microwave Limeil offer for 3 V radiocommunication applications.

This offer includes low cost, plastic packaged 27 dBm 1800-1900 MHz and 32 dBm 900 MHz power amplifiers, to be sampled in 1994.

This product range will evolve in 1995 towards integrated Rx/Tx front ends, which monolithically integrate the low noise stages of the Rx chain at a marginal cost, in terms of semiconductor area.

Acknowledgements

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