A New SPICE-Type Heterojunction Bipolar Transistor Large-Signal Model

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Abstract: A new SPICE-type, HBT large-signal model is described with special emphasis on the associated parameter extraction techniques. The model can be used to simulate HBT's under DC, microwave small-signal and large-signal conditions. Also, allowance is made for self-heating effects, which are quite pronounced in HBT's. Excellent agreement between measured and simulated results demonstrate the utility of the proposed model in large-signal design.

I. Introduction

Microwave circuit designers ideally require a unified heterojunction bipolar transistor (HBT) circuit model, which is valid for DC, microwave small-signal and large-signal operation. Conventional BJT models such as Ebers-Moll or Gummel-Poon are often used to model HBT's, since both kinds of transistor share similar operating principles [1-7]. The difficulty with this approach is that it generally results in models with only restrictive regions of application, since HBT's actually present several significant differences in behaviour compared to Silicon BJT's, and these differences cannot properly be represented within traditional BJT models [9]. Existing HBT models are often only valid for DC or small-signal AC conditions, although they can be extended somewhat using Volterra series techniques to simulate the device at medium input signal power levels and at a fixed bias point. The present contribution arises from the development of a general-purpose HBT model which can cover DC, small-signal AC and microwave large-signal applications. The model itself is described in more detail in [8]: here we emphasise the associated parameter extraction techniques.

II. Background to Model Development

The main problems related to HBT modelling include: (i) non-uniform current gain which is caused by strong recombination currents in the Space Charge Region (SCR) and on the interface of the heterojunction; (ii) non-linear charge storage in the emitter, base and base-collector SCR which depend on the bias condition; (iii) self-heating effects which arise due to the HBT's high power density. These effects cannot be included in conventional BJT models in a simple way. This paper is based on a new HBT description which is different from conventional Ebers-Moll or Gummel-Poon models and is, in essence, a semi-experimentally based model. The main features of the proposed model may be listed as follows: (1) It is intended to be valid for all applications from DC to large-signal microwave. This feature is very important when a high amplitude microwave signal is applied to the input of the HBT, since the bias point usually then varies with the signal level. The resulting variations in current gain, junction temperature, etc., feed back to influence the bias point itself. Only a model which correctly predicts DC characteristics can be used to predict accurately the large-signal AC performance. Models based on Volterra Series analysis, for example, do not have this feature [5,7]. (2) Self-heating effects are included in the new model. This means that model parameters can be dynamically modified by the junction temperature. Whenever a signal is added to the HBT, the thermal subcircuit can calculate junction temperature and modify model parameters instantly. For AlGaAs/GaAs HBT's the thermal effect is very important and causes a negative slope in output characteristics. (3) The proposed model gives rise to a very simple parameter extraction process which involves a series of straightforward measurements including DC and wide-band (CW) S-parameters. As the parameter extraction process is considered here to be a critically important aspect of using the model in practice, it is described in some detail in Section IV below.

III. New HBT Non-linear Model

The HBT model under discussion here is shown in Fig. 1 [8]. Note that a change in the standard topology has been introduced, involving a splitting up of the base region into several nodes. Two non-linear resistors are used to simulate the base and collector current deviation from ideal exponential behaviour under high-current operation. Diode D_{BE_Ib} is used to simulate the base-emitter current which has an ideality factor of n_{BE_Ib} in the low-to-medium current region. Diode D_{BE_Ic} is used to simulate the collector current dependence on V_{BE} and has an ideality factor $n_{BE\_Ic} < n_{BE\_Ib}$ in the same region. For D_{BE_Ib} and D_{BE_Ic}:

$$I = I_{S\_ib}(T_j)\cdot\left(e^{\frac{V}{n_{be\_ib}(T_j)\cdot V_T(T_j)}}-1\right) \qquad (1)$$

$$I = I_{s\_ic}(T_j)\cdot\left(e^{\frac{V}{n_{be\_ic}(T_j)\cdot V_T(T_j)}}-1\right) \qquad (2)$$

where V and I are the voltage and current applied to the diode ports, and Tj is the temperature of the junction. Temperature-dependence in the diode characteristics is introduced by equations (3 & 4) below for the saturation current and the ideality factor. Here, T_0 is room

temperature and Tj is the *computation junction temperature*. The latter term is used here as distinct from the real junction temperature, which at some particular points in the device might differ from the real junction temperature.

$$I_s(T_j) = I_s(T_0) \cdot e^{\left(\frac{1}{T_0}-\frac{1}{T_j}\right)\cdot T_s} \quad (3)$$

$$n(T_j) = n(T_0) \cdot \left(1 + A_n \cdot \Delta T + B_n \cdot \Delta T^2\right) \quad (4)$$

The *computation junction temperature* is a tool to connect the dissipated power inside the HBT with the electrical behaviour of the device. D_{BC} is used to simulate the normal BC homojunction. A simple thermal sub-circuit is used to calculate the temperature of the junction, and enables the model to take account of self-heating effects in the device. The dynamic part of the model is simulated by a nonlinear charge component Qb which represents the mobile charge storage in the different regions of the HBT. When the device is forward-biased, the capacitances related with this charge are the diffusion capacitance for the BE junction and the depletion capacitance for the BC junction. Since some physical parameters such as base width and BC junction SCR width are the functions of Vbc, the charge is also modulated by Vbc. In order to construct Qb, a simple approximate function which is obtained from a simple physical analysis is used to curve-fit the measured small-signal data (multi-bias S-parameters) in the forward bias region:

$$Q_b = f(V_{be}, V_{bc}) \quad (5)$$

For the simplest case, the charge can be assumed to be partitionable and represented as Cbe and Cbc. The new model is a quasi-static model and the carrier-transit time delay has been included into the charge term.

IV. Parameter Extraction Techniques

The end-user of a model must also know how to extract the parameters of that model correctly. In general, there are two basic approaches available to do this. Firstly, through the use of advanced optimisation techniques, the model parameters can be adjusted to fit measurement results. When a good fit has been achieved for all measurements over all operating conditions of interest, the result is a set of parameters which can be used by circuit designers. Recently, several software packages based on this approach have become widely used. The main problem associated with this method is that a physically-unrealistic solution can occur due to the presence of many local minimum solutions. An alternative approach is based on performing a specially-designed group of sequential measurements, accompanied by direct extraction of model parameters through suitable processing of the resultant data [9]. In the authors' opinion, the model parameter extraction process is as important as the model itself, and the best way to perform parameter extraction is through a combination of the above two methods, aiming at a reduction to a minimum of the number of optimisation variables involved, thereby avoiding the multi-solution problem and also saving on computation time. Since the proposed model is basically formed by diode equations and resistance elements within the framework of the new topology, the parameter extraction process becomes very simple. The steps are as follows:

A: Perform the necessary forward and reverse measurements to obtain Gummel-Plots. This measurement can be performed with Vbc=0 (forward) and Vbe=0 (reverse).

B: From the forward Gummel-plot, the two straight lines on the log-linear plot in the medium-current region give I_{S_Ib}, I_{S_Ic},, n_{BE_Ib} and n_{BE_Ic} directly by graphical methods as shown in Fig. 2.

C: From the reverse Gummel-Plot, I_{S_BC} and n_{BC} can be extracted by a similar method.

D: The emitter resistance is determined by using the open-collector method [9] as shown in Fig. 3.

E. The collector resistance can be obtained by directly observing the slope of the collector output characteristics as shown in Fig. 4.

F. Observing the deviations of Log(Ib) and Log(Ic) from the ideal straight line on the Gummel plot, we find that $\Delta(V_{ib})$ and $\Delta(V_{ic})$ for a given base-emitter voltage, are generally not equal for the HBT as one would expect for a normal BJT (see Fig. 5):

$$\Delta(V_{ib}) = n_{be\_ib} \cdot V_T \ln\left(\frac{I_{b\_ideal}}{I_{b\_test}}\right) = R_{bx} \cdot I_b + R_{bi\_ib} \cdot I_b + R_e \cdot I_e \quad (6)$$

$$\Delta(V_{ic}) = n_{be\_ic} \cdot V_T \ln\left(\frac{I_{c\_ideal}}{I_{c\_test}}\right) = R_{bx} \cdot I_b + R_{bi\_ic} \cdot I_c + R_e \cdot I_e \quad (7)$$

For $\Delta(V_{ib}) < \Delta(V_{ic})$, the nonlinear resistance Rbi_ic is used to compensate for this difference, with Rbi_ib=0. The values of Rbx and Rb_ic are extracted by using the following expressions:

$$R_{bx} = \frac{\Delta(V_{ib}) - R_e \cdot I_e}{I_b} \quad (8)$$

$$R_{bi\_ic} = \frac{\Delta(V_{ic}) - \Delta(V_{ib})}{I_c} \quad (9)$$

For $\Delta(V_{ib}) > \Delta(V_{ic})$, the small resistance Rbi_ib is used for compensation, with Rbi_ic set to zero, and Rbx and Rbi_ib are extracted using equations 10 & 11. Normally these resistances are nonlinear functions of the base and collector currents, but we can set Rbx constant since it is mainly a contact resistance. Rbi_ib

and Rbi_ic strongly depend on the bias point because they are modulated by the carrier concentration in the intrinsic base region.

$$R_{bx} = \frac{\Delta(V_{ic}) - R_e \cdot I_e}{I_b} \qquad (10)$$

$$R_{bi\_ib} = \frac{\Delta(V_{ib}) - \Delta(V_{ic})}{I_b} \qquad (11)$$

G. The *computation thermal resistance* can be extracted after extraction of all the other DC parameters. The thermal resistance value is adjusted to make the output characteristics of the simulation fit the measured characteristics and to obtain the same negative slope in the high current region.

H. The base charge component Qb can be extracted after extraction of all the DC and thermal parameters. At this stage all the DC parameters are fixed and the model can give correct DC characteristics at all bias points. The broadband small-signal S parameters of the device are measured at numerous bias points in the forward bias plane to form a net or grid which covers the entire desired region of operation. The two capacitances of the model can then be optimised to make all four S parameters fit the measurement results, giving the two capacitances as functions of the bias applied. Because only two variables are involved in this optimisation process, a unique solution can be achieved relatively easily. After Cbe(Ic, Vce) and Cbc(Ic, Vce) are obtained, a formula based on the semiconductor analysis is used to curve-fit these capacitances. Then the Qb can be obtained by:

$$Q_b = \int_0^{V_{be}} C_{be}(\xi, 0)\, d\xi + \int_0^{V_{bc}} C_{bc}(V_{be}, \eta)\, d\eta \qquad (12)$$

Thus, the whole parameter set can be extracted from the above process step-by-step, by performing DC and broadband small-signal S parameters measurements and some simple optimisation. This gives us a quasi-static model where time delay is included in the charge model.

V. Verification of the New HBT Model

The full parameter extraction process has been carried out for several different AlGaAs/GaAs HBTs obtained from Siemens and Rockwell. We have used the parameters extracted by our method to simulate the DC performance and then compared with measured results (Fig. 6). Very good agreement is obtained. For the same parameters and model, we use HP-MDS to generate the small-signal S parameters, and these are compared with the measurement results and show good agreement at all bias points. The final and most important step in verifying the model is through the use of a 50Ω power sweep measurement. Since all the model parameters are extracted from DC and broad-band S-parameter measurements, the power sweep is an independent method of large-signal verification. In fact, the measured and simulated results are found to show excellent agreement, as shown in Fig. 7 for a Siemens HBT, and Fig. 8 for a Rockwell HBT.

VI. Conclusions

A new HBT large-signal model has been developed which includes self-heating effects. The model is based on experimental observation and physical analysis which leads to a very direct parameter extraction process, as described in this paper. The introduction of a new topology to split the base into several regions allows the base and collector currents to be tracked very accurately. A thermal sub-circuit which includes a simplified *computational thermal resistance* and *computational thermal capacitance* allows effective simulation of self-heating effects. This model is a practical model and can be added to commercial software products and SPICE without difficulties.

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References

[1] M. E. Kim, A. K. Oki, G. M. Gorman, D. K. Umemoto, J. B. Camou, "GaAs heterojunction bipolar transistor device and IC technology for high-performance analog and microwave application," IEEE Trans. MTT., Vol. 37, pp. 1286-1303, September 1989

[2] M. E. Hafizi, C. R. Crowell, M. E. Grupen, "The DC characteristics of GaAs/AlGaAs heterojunction bipolar transistors with application to device modeling," IEEE Trans ED, Vol. 37, pp. 2121-2129, Oct. 1990

[3] M. Y. Frankel, D. Pavlidis, "An analysis of the large-signal characteristics of AlGaAs/GaAs heterojunction bipolar transistors," IEEE Trans. MTT, Vol.40, pp.465-474, March 1992

[4] D. A. Teeter, J. R. East, R. K. Mains, G. I. Haddad, "Large-signal numerical and analytical HBT models," IEEE Trans. ED, Vol.40, pp.837-845, May 1993

[5] S. A. Maas, B. L. Nelson, D. L. Tait, "Intermodulation in heterojunction bipolar transistors," IEEE Trans. MTT, Vol.40, pp.442-448, March 1992

[6] P. Grossman, J. Choma, Jr, "Large-signal modeling of HBT's including self-heating and transit time effects," IEEE Trans MTT, Vol.40, pp.449-464, March 1992

[7] A. Samelis, D. Pavlidis, "Mechanisms determing third order intermodulation distortion in AlGaAs/GaAs heterojunction bipolar transistors," IEEE Trans MTT, Vol.40, pp.2374-2380, 1992.

[8] K. Lu, P. Perry, T. J. Brazil, "A new SPICE-type heterojunction bipolar transistor model for DC, microwave, small-signal and large-signal circuit simulation," To be published in MTT-S, 1994.

[9] Getreu, I. E.: "Modeling the bipolar transistor" Tektronix, Beaverton, 1976.

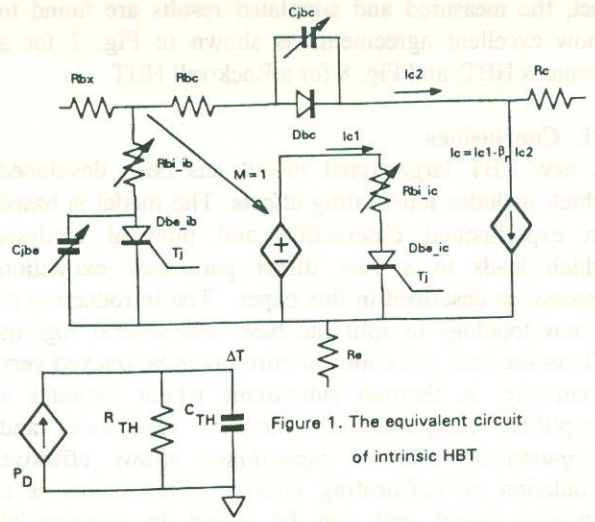

Figure 1. The equivalent circuit of intrinsic HBT

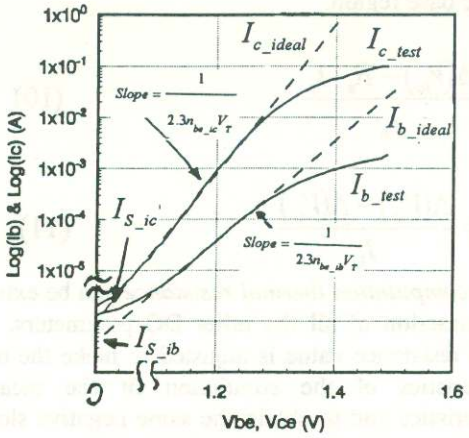

Figure 2 Gummel plot for an HBT showing graphical extraction of saturation currents and ideality factors

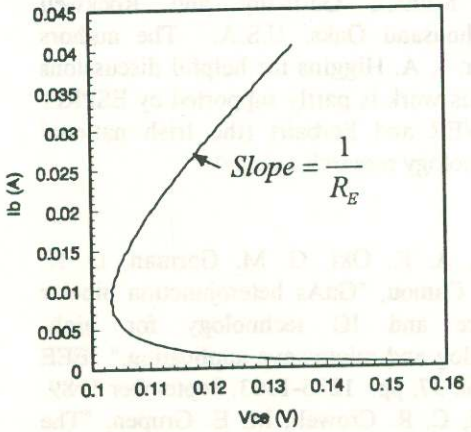

Figure 3 Open-collector measurement result showing graphical extraction of Re

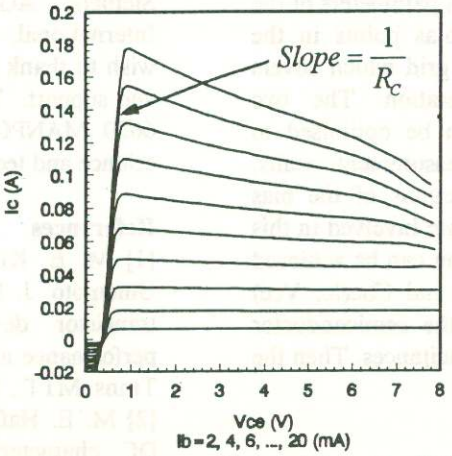

Figure 4 Output characteristics of an HBT showing graphical extraction of Rc

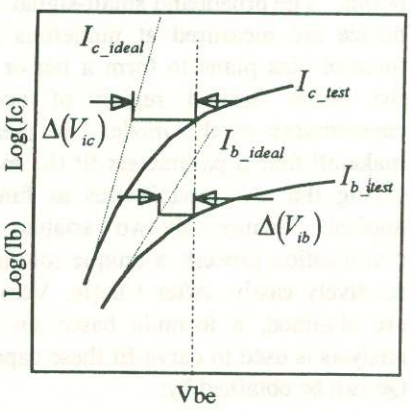

Figure 5 Gummel plot of an HBT in high current region showing the difference between $\Delta(V_{ib})$ and $\Delta(V_{ic})$

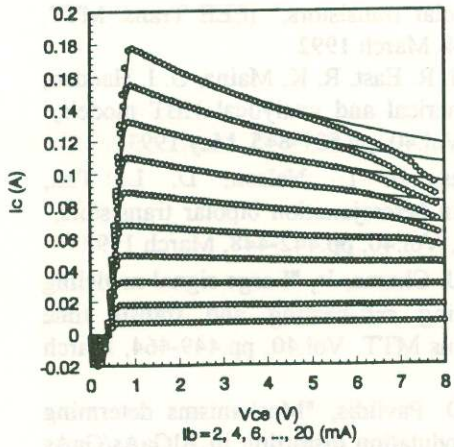

Figure 6. Measured (circles) and simulated (solid line) DC output characteristics of a Siemens HBT

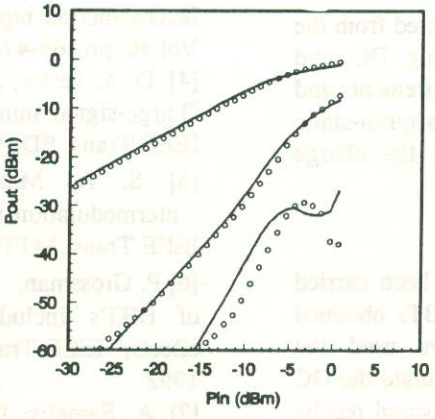

Figure 7. Comparison of measured (circles) and simulated (solid lines) first three harmonic components for Siemens HBT

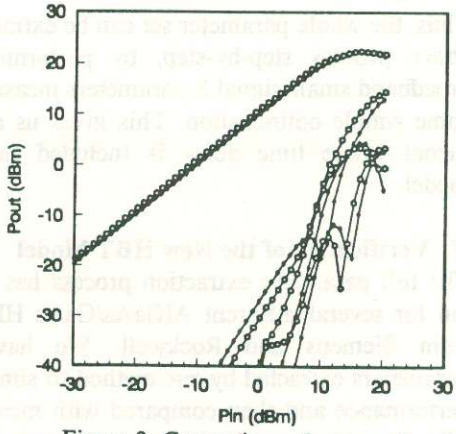

Figure 8. Comparison of measured (circles) and simulated (diamonds) first four harmonic components for Rockwell HBT