A FAMILY OF HIGH SPEED DIGITAL GaAs GATE ARRAYS WITH AN APPLICATION FOR 432 MBIT/S SYNCHRONOUS TRANSMISSION

Laurent Boganski *, Erwan Froc ** and Henri Fourdeux **

* Thomson Composants Microondes Orsay France
** Thomson CSF Laboratoires d'Electronique de Rennes France

ABSTRACT

A GaAs gate array family is fabricated with Thomson Composants Microondes Self Aligned Gallium Arsenide process with 0.8 μm Leff E/D MESFETs, 3 metal layers on 4" wafers. The complexity ranges from 3.000 to 30.000 DCFL 2 inputs NOR gates. The unloaded gate delay is 70 ps with a power of 0.3 mW. Two personnalizations of the 3K array have been designed by the Laboratoire d'Electronique de Rennes for an HDTV system. They consist in 11:1 serializer and 1:11 deserializer with a throughput of 432 MBit/s.

1 PROCESS

The process is based on Enhancement-mode and Depletion-mode MESFETs with refractory metal self aligned Shottky-barrier gates. The GaAs wafer are 4 inches. The devices are interconnected with standard aluminium interconnect processing technology. A process cross-sectional view is shown in figure 1. First, the channel regions are formed with ion implantation. Next, gate metal is used to form self-aligned ion implanted N+ source and drain regions. The effective gate length is 0.8 μm. Ohmic contacts are then deposited to make an electrical connection to the source and drain implants.

Finally, the three metal layers are made with aluminium using standard silicon processing techniques. The nominal threshold voltage are 0.25 V for the enhancement-mode MESFETs and -0.8 V for the depletion-mode MESFETs. The process requires only 11 masks steps, which is less than half the number of levels required for a standard silicon ECL or BiCMOS process.

This process and gate-array family has been developed by Vitesse Semiconductor Corporation [1] [2], and transferred to Thomson Composants Microondes for second-sourcing.

2 TGAII GATE ARRAYS FEATURES

2.1 Cell design

The gate arrays of the TGAII family contain from 3.584 to 30.584 cells. A cell is an unbuffered 2-input NOR gates, constituted of one D-mode MESFET and two E-mode MESFETs. The cells are grouped in pairs to form a MAU or Minimum Addressable Unit, which is shown in figure 2. These Direct Coupled Fet Logic NOR gates are similar to silicon E/D NMOS except for the Schottky diode gate that clamps the logic high voltage. The voltage swing magnitude is identical to ECL, but DCFL operates with only a 2 volt power supply. The power dissipation is less than half that of ECL for the same power supply current and same speed. Because of the Schottky diode clamp, a constant current is drawn from the power supply. Therefore DCFL exhibits no frequency dependent power as does CMOS or BiCMOS. Power dissipation per core cell is typically 0.3 mW. The typical unloaded gate delay is 70 ps. The maximum clock to output delay for a positive edge triggered D flip-flop is 424 ps. The maximum toggle frequency is about 1 GHz with 0.5 mm wire load.

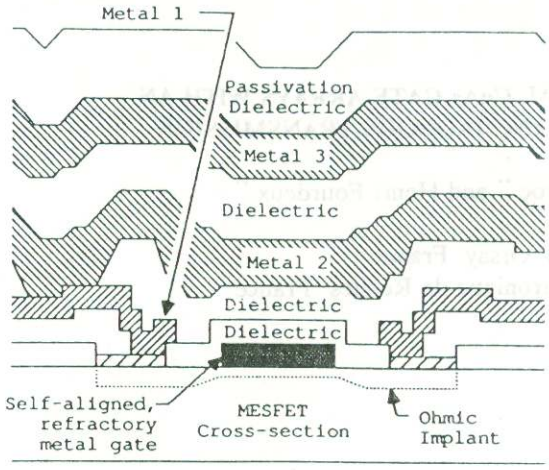

Figure 1: *MESFET Cross-Section*

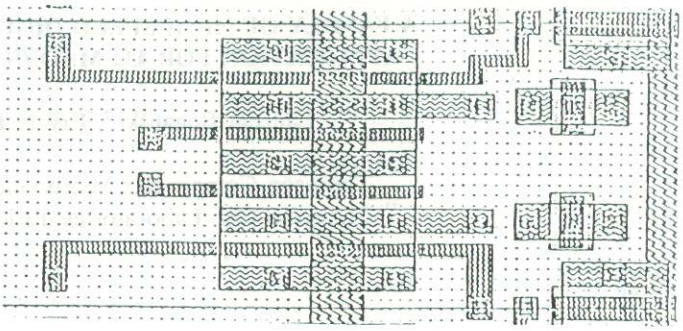

Figure 2: *Core cells layout*

2.2 Gate arrays architecture

The arrays are channelled as seen on figure 3. Macro-cells are designed in metal 1 over the rows. Signal routing is accomplished in metal 1 and metal 2. Metal 3 is dedicated to global power bussing.

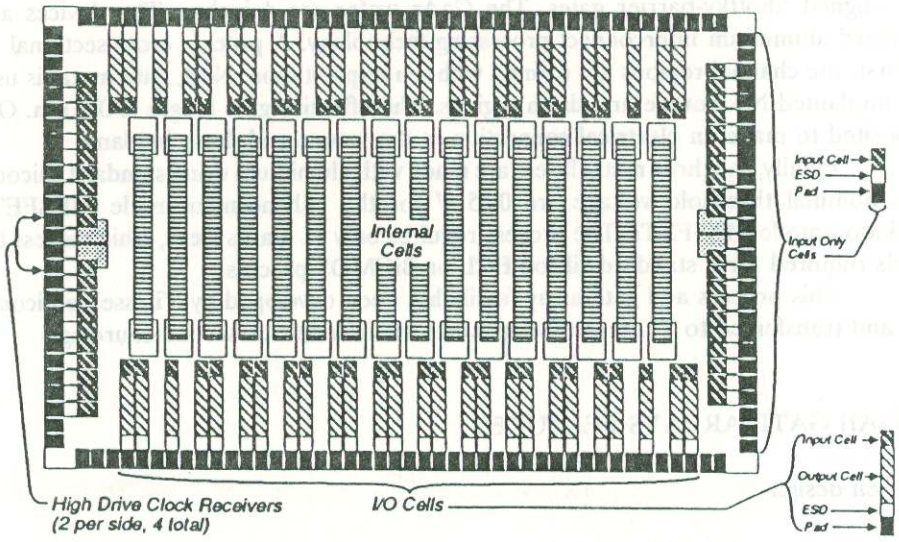

Figure 3: *3K array structure*

The inputs and outputs can be personalized for TTL, ECL or GaAs voltage interfaces. The gate arrays provide two types of I/Os: input-only cells and combination input-output cells.
The input cells contain ESD protection diodes and one can select a variety of input personalization options. The input cell provides a receiver plus other configurable logic such as a latch, flip-flop, multiplexer or buffer. The input-only sides of the arrays contain clock driver cells, which are six times larger than the standard input receivers, in order to drive high frequency clock trees. These clock buffers are located on the input-only edges of the arrays, away from the noise of the outputs on the other edges of the arrays.
The I/O cells are located on the longest sides of the periphery of the arrays. The I/O cell can be used for

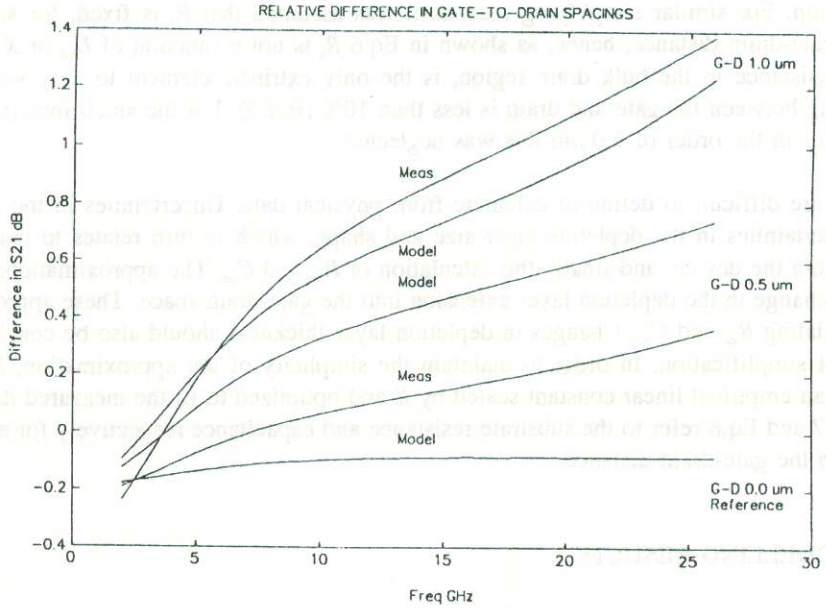

Figure 2: ***Magnitude of empirical versus physical modelled S_{21} data for gate-drain distance increases of 0.5 and 1.0 μm, normalized to a standard reference device.***

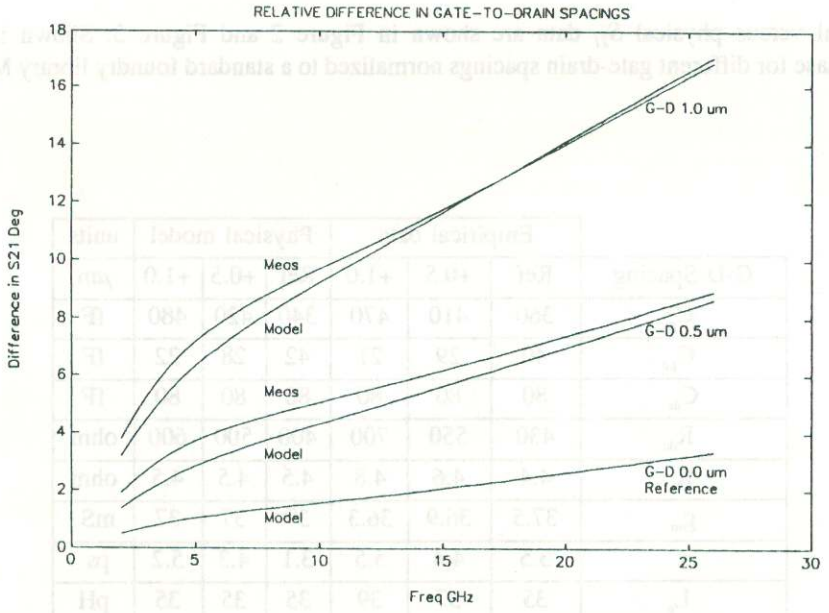

Figure 3: Phase of empirical versus physical modelled S_{21} data for gate-drain distance increases of 0.5 and 1.0 μm, normalized to a standard reference device.

Two sets of measurement comparisons of discrete device were made. The first is of a standard MESFET and a MESFET with a gate-drain distance increase of 0.5 μm, which shows, at 20 GHz, a phase difference of approximately 7 degrees with less than a 0.6 dB gain difference. The second is of a standard MESFET and a MESFET with a gate-drain distance increase of 1.0 μm, which shows, at 20 GHz, a phase difference of approximately 14 degrees with less than a 1.2 dB gain difference.

input-only, output-only, bidirectional interface. The cell contains a receiver section with optional logic, an output driver with optional logic and ESD protection.

2.3 The family of arrays

Table 1 shows the different sizes and features of the arrays.

Array Name	# of internal gates		# of I cells		# I/O cells	Output Only Cells	Total Signal Pins (1)	Package Options
	Total Cells	NOR2 / DFF	TTL,ECL GaAs	Hi-Drive	TTL ECL GaAs			
TGAII3K	3.584	3.584 / 290	40	4	52	-	92	52LDCC 132LDCC
TGAII5K	6.400	6.400 / 520	52	4	68	-	120	149PGA 164LDCC
TGAII10K	13.376	13.376 / 1.100	74	8	100	-	174	211PGA
			96	8	100	-	196	256LDCC
TGAII15K	16.896	16.896 / 1.408	74	8	100	-	174	211PGA
			96	8	100	-	196	256LDCC
TGAII20K8R (2)	20.736	20.736 / 1.728	96	8	132	19	256	344LDCC
TGAII30K	30.528	30.528 / 2.544	100	8	156	-	256	344LDCC

(1) Excluding power supply pins

(2) RAM array includes 8Kbits SRAM : (256x4)x8

Table 1: *Array family features*

2.3 Design flow

The gate array designs follow an established flow based on experience of VITESSE™. The standard design flow is:

.Front-end: design feasibility and specifications review, schematic entry, at-speed and functional (for test) simulations with front-annotation, preplacement of critical paths.

.Back-end: place and route, back-annotated simulations, critical design review.

Designs are supported on most major workstations: MENTOR ™, VALID ™, DAISY ™, VERILOG ™. SYNOPSYS ™ Logic synthesis tool is also supported, which will provide a speed-optimized gate implementation for behavioural level circuit description to a logic simulator. A variety of custom software programs have been developed to help with the above design flow.

3 IMPLEMENTATION OF SERIALIZER AND DESERIALIZER

3.1 Presentation

Two circuits have been studied and designed at Thomson-CSF/ Laboratoires d'Electronique de Rennes. Both are based on TGAII3K arrays using Thomson Composants Microondes SAGA08 self-aligned Gallium Arsenide process. These circuits are a serializer and a deserializer with a serial throughput designed for single medium transmission. The serial data can be transmitted through a coaxial cable or converted to light pulses for transmission through an optical fibre up to 500Mbit/s.

3.2 Using environment

These ASICs have been designed to ensure serial/parallel interconnections between equipment and inside equipment in a High Definition Television Digital studio. They perform the serialization and deserialization of the Y1, Y2, Cr, Cb video components (10 parallel synchronous signals at 36Mbit/s throughput) before and after the transmission. The digital serial signal is sent out on a single medium. To simplify the reception of the signal, a specific line coding must be used to give the following properties to the signal:
- average value Ao constant and equal to A/2 (A is the peak to peak amplitude of the received data).
- high transition density
- number of binary digits (consecutively set to 0 or 1) as low as possible.

Several code systems meet these requirements [3]. The chosen code is a 2* (5 scrambled bits + 1 complementary bit). For high speed transmission, transition enhancement is provided by the scrambler [4], which guarantees sufficient transitions to ensure the proper operation of timing recovery system. The complementary bits are benefit to clock recovery and also permit to achieve the synchronization without any synchronization word, thus the transmission is independent of the data's content.

3.3 Serializer

The serializer (figure 4) accepts a maximum of 11 data inputs, fully compatible with TTL levels. For the latter application ten video inputs and an optional input for audio or control signals are used.
The serializer is made of five blocks shown in figure 1. The first block contains a programmable frequency divider generating the parallel clock and the multiplexer load control. The second one ensures the coding function by data scrambling and adding of complementary bits; this operation is made at the parallel data rate. the resulting 12 coded parallel data are sent to the temporal multiplexer block. At last a NZR/NZRI encoding can be carried out if selected.
The chip also integrates a phase-frequency comparator which can be included in a phase locked loop to generate the master frequency. Several serial data streams are available with ECL compatible outputs (figure 6). They allow 50 Ohms and 25 Ohms loads, differential outputs are also available.
The voltage controlled oscillator and the loop filter are off the chip, they are implemented on the serializer's module.
A further chip version will integrate a fully internal PLL. Such a solution should decrease power consumption and serializer's board size.

3.4 Deserializer

At the receiving end, the deserializer (figure 5) performs the dual serializer's function, i.e. data descrambling, temporal demultiplexing and data synchronisation. The synchronisation system runs at the parallel clock rate, it is designed to keep a good synchronisation despite transmission errors possibly introduced by the transmission channel. The chip is implemented on a deserializer module which also performs a signal reshaping of the data: amplitude decision, clock recovery, time decision.
Parallel data are available with TTL compatible levels (figure 7).

3.5 Characteristics

The serializer and the deserializer circuits are integrated in TGAII3K arrays using Direct Coupled FET Logic. They use SAGA08, self aligned Gallium Arsenide process with 0.8 μm effective length E/D MESFETs. Both are packaged in 52LDCC quad flatpack.
They need standard power supplies: -2V for the internal logic core and the ECL input/output buffers, +5V for the TTL I/O buffers. A Vbb = -1.32V external reference voltage is used to improve noise margins on sensitive ECL inputs.
Their respective complexity is 1970 and 2660 equivalent NOR gates for the serializer and the deserializer and their respective typical power consumption is 0.83W and 1.1W. These values are confirmed by experimental measurements. The low power consumption is achieved by the use of a multilevel bufferization logic gates. The quite low consumption associated with the good thermal properties of the package enable the two circuits to run without any heat-sink within the commercial temperature range 0°C-70°C.

3.6 Application

These circuits have been designed to allow the implementation of a broad range of transmission systems. The line coding property is such that the circuits are completely transparent with respect to data to transmit. They are polyvalent and can be used to transmit any kind of data independently of their content. The data have just to respect a 11 line parallel data format or less, up to 42 Mbit/s rate, the resulting throughput is up to 500 Mbit/s.
It is also possible to couple two serializers and two deserializers for doubling the input format, the bit stream recognition is easily done by specific coding for each of them.
Two modules with the ASICs and their environment are available to implement such function.

4 REFERENCES

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[2] R. Hinds, S. Canaga, G. Lee, A. Choudury, *A 20K GaAs array with 10K of embedded SRAM*, 1990 CICC Proceedings pp 4.5.1-4.5.4
[3] H. Fourdeux - C. Claverie, *Digital HDTV transmission on optical fibre*, IBC Conference 1988 pp 280-283
[4] J.E. Savage, *Some simple self synchronizing digital scramblers*, Bell Syst. Tech. J Vol 42 pp 449-487

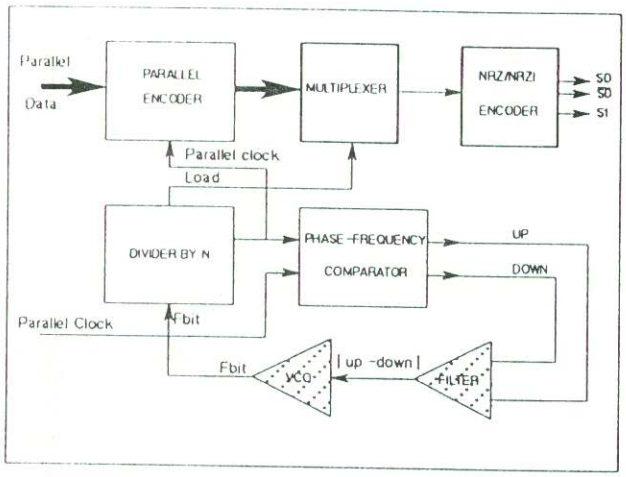

Figure 4: *Serializer Block diagram*

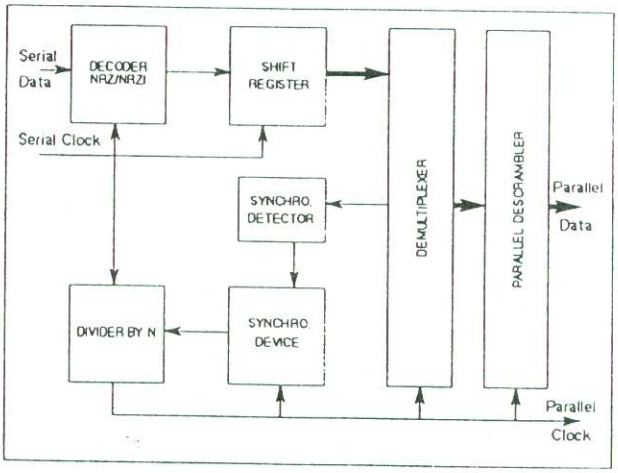

Figure 5: *Deserializer Block Diagram*

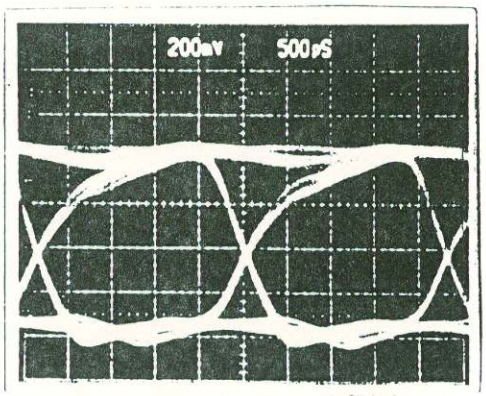

Figure 6: *432 Mbit/s ECL Output*

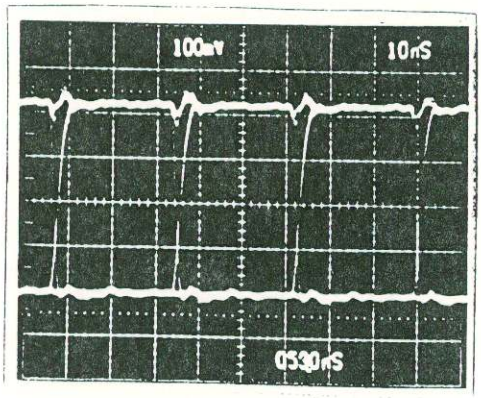

Figure 7: *36 Mbit/s TTL output*