

1W/mm GaAs pHEMT for realization of linear power amplifier in the K band.

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Abstract

The realization and characterization of $\text{Al}_{0.22}\text{Ga}_{0.78}\text{As}/\text{In}_{0.22}\text{Ga}_{0.78}\text{As}/\text{GaAs}$ power pHEMT are reported. This structure was optimized to obtain a quasi flat transconductance profile to increase the device linearity near the compression. A maximum single carrier output power higher than 0.8 W/mm for 2 dB compression has been obtained, with more than 30 % power added efficiency and 7.4 dB linear gain at 18.5 GHz. Two tones intermodulation distortion have shown a C/I ratio of 19.9 dBc and 42.3 dBc to the 3rd and 5th order respectively, for an input two tones power corresponding to 1 dB compression input power in CW.

I. Introduction

Nowadays, applications like multimedia telecommunications know a very important expansion in the world. So, the development of linear power amplifiers, in the K and Ka bands, arouses a lot of interests. To reduce third order intermodulation distortion generated by power amplifiers, it is necessary to limit the device nonlinearities by optimizing the transistor structure.

The AlGaAs/InGaAs pHEMT has demonstrated its capability to obtain at 30 GHz a 1 W/mm power density^[1] and 30 to 40 % power added efficiency. This original work was based on a two channels GaAs pHEMT. This structure allows a high drain current value and a quasi flat transconductance profile. These two parameters are a key point to get high power and high linearity simultaneously.

In the first part, this contribution presents the technology of the device we have designed and realized. The second part reports DC and RF device characterization, including small and large signal measurements. And the last part concerns the linear power amplifier conception and characterization, with power and intermodulation performances at 18.5 GHz.

II. Device Processing

The pHEMT structure used in this study (figure 1) was grown by solid source molecular beam epitaxy. The epilayer has been optimized using 1D modeling software based on Schrödinger - Poisson equation resolution. Our optimization criterion is the charge command control linearity. The structure consists of a 70 nm n^+ GaAs cap layer with a doping level of 5.10^{18}cm^{-3} , a 20 nm undoped $\text{Al}_{0.22}\text{Ga}_{0.78}\text{As}$ Schottky barrier, a first Si δ -doping (4.10^{12}cm^{-2}) with an undoped GaAs channel followed by a second Si δ -doping (4.10^{12}cm^{-2}) with an undoped $\text{In}_{0.22}\text{Ga}_{0.78}\text{As}$ channel.

In our application, we need the maximum of aluminum concentration in the high band gap layer to obtain a good electron confinement in the channel, a high barrier discontinuity and a better

control of the gate recessing because the selectivity between GaAs and AlGaAs increases with the aluminum concentration. But in the case of an important Al mole fraction, problems could appear due to DX centers. So, we have chosen an Al mole fraction of 22 % to minimize these problems.

The process started with device isolation through mesa etching. The Ni/Ge/Au/Ti/Au ohmic contacts were annealed at 400°C during 40 s. A contact resistance of 0.07 Ω .mm is obtained. The 0.2 μm centered gates are defined by electron beam lithography. The gate recessing is performed using citric acid/hydrogen peroxide/ammonium hydroxide solution^[2] we have developed to take advantage of the high selectivity between GaAs and AlGaAs and minimize the nonlinearities due to the gate recessing. Ti/Pt/Au is evaporated for the gate metallization. A 500 \AA Si_3N_4 film is deposited to passivate the device and to minimize the effects of electrical stress on the gate breakdown voltage.

III. Device Characterization

The I-V static characteristics of a 6x50x0.2 μm^2 pHEMT show a maximum drain current value of 800 mA/mm. The pinch-off and the breakdown voltages are -3 V and 7 V respectively. As it can be seen on the figure 2, the evolution of the transconductance profile is quasi flat over a large gate source voltage of more than 2 V with two maxima, in agreement with 1D Schrödinger-Poisson simulation. The maximum DC extrinsic transconductance value (350 mS/mm) is obtained at $V_{\text{gs}} = 0.1$ V while the maximum RF intrinsic value (430 mS/mm) is obtained at $V_{\text{gs}} = -1.9$ V.

Very low electrical dispersion was obtained on the wafer processed. Standard deviation values of 39 mA/mm and 32 mV have been obtained respectively for the drain current density and the pinch-off voltage, due to the development of a high selective citric acid solution we have used to perform the gate recess.

Single carrier power measurements have been performed on a passive load pull system using two manual tuners. The evolution of output power, gain and power added efficiency versus input power at 19 GHz are shown in figure 3. An output power of 1W/mm has been obtained at 1 dB compression with 30 % power added efficiency and 9 dB linear gain, for $V_{\text{ds}} = 5$ V and V_{gs} corresponding to the maximum of transconductance value.

IV. Linear Power Amplifier

The power amplifier consists of a single stage power pHEMT amplifier with a total gate width of 6x50 μm . The amplifier has been simulated by using HP Eesof Libra software.

Figure 4 shows the output power response of the linear power amplifier at 18.5 GHz, in single carrier mode, for a drain source and a gate source voltage of 4 V and -1.5 V respectively. In these conditions, an output power of 23.9 dBm (820 mW/mm) has been measured for 2 dB compression with 31 % power added efficiency and 7.4 dB linear gain.

Two tones intermodulation measurements indicated a maximum 3rd order intercept point (IP_3) of 34 dBm in agreement with Libra simulations. The difference between IP_3 and $\text{PS}_{1\text{dB}}$ values is higher than 10 dB which can confirm the good component linearity for a classical transistor^[3]. But in our case, this linearity factor can't be used, because the structure is optimized to increase the linearity near the compression and not at low input power.

Two tones C/I intermodulation measurements have been reported in the figure 5 in the case of $F_1 = 18.5$ GHz and $F_2 = 18.51$ GHz for the same V_{ds} and V_{gs} polarization. The 3rd and 5th order C/I ratio decreases as P_e increases but between 1 and 2 dB compression we can see a raise of the $(\text{C/I})_5$ with a maximum value of 45 dBc. For an input two tones power corresponding to 1 dB compression input CW power, a $(\text{C/I})_3$ and a $(\text{C/I})_5$ of 19.9 dBc and 42.3 dBc respectively have been obtained. These results are better than what has been reported in the literature^[4]. In table 1, we can see a comparison of intermodulation products between different classical structures (MESFET and conventional pHEMT) and our study. The optimized pHEMT structure presents the same linearity for low output power but a linearity higher than 5 dB at the $\text{PS}_{2\text{dB}}$.

The figure 6 reports the Gain, Ps, PAE and C/I evolutions versus Vgs for Vds = 4 V, $P_{e1} + P_{e2} = P_{e1dB}$ (CW) and F = 18.5 GHz. The 3rd and 5th order C/I ratio are higher than 19.3 dBc and 39.3 dBc respectively over a large gate source voltage range. In these conditions, the gain, Ps and PAE are better than 7 dB, 500 mW/mm and 23 % respectively.

V Conclusion.

The realization and characterization of linear power pHEMT are reported. The transconductance profile has been optimized over the Vgs polarization to increase the linearity near the compression. An output power of 1W/mm has been obtained at 1 dB compression. This pHEMT structure has been used in the conception and the realization of a single stage linear power amplifier. Power measurements indicate the capability of this device to obtain an output power in single carrier mode higher than 800 mW/mm at 2 dB compression and a PAE better than 30 % with 7.4 dB linear gain. Intermodulation measurements have shown a 3rd and 5th order C/I ratio higher than 19.3 dBc and 39.3 dBc over a large gate source voltage range. These results confirm the good capabilities of this device to get simultaneously high power density and high linearity.

Références

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GaAs	5.10^{18}cm^{-3}	70 nm
AlAs		0.5 nm
$\text{Al}_{0,22}\text{Ga}_{0,78}\text{As}$		20 nm
GaAs		0.4 nm
δSi	4.10^{12}cm^{-2}	
GaAs		0.4 nm
$\text{Al}_{0,22}\text{Ga}_{0,78}\text{As}$		3 nm
GaAs		12 nm
AlAs/GaAs 6x		5 nm
δSi	4.10^{12}cm^{-2}	
GaAs		0.4 nm
$\text{Al}_{0,22}\text{Ga}_{0,78}\text{As}$		2 nm
GaAs		1 nm
$\text{In}_{0,22}\text{Ga}_{0,78}\text{As}$		12 nm
GaAs		1.5 nm
$\text{Al}_{0,22}\text{Ga}_{0,78}\text{As}$		150 nm
GaAs		300 nm
AlAs		30 nm
GaAs substrate		

Figure 1 : Schematic of the pHEMT structure

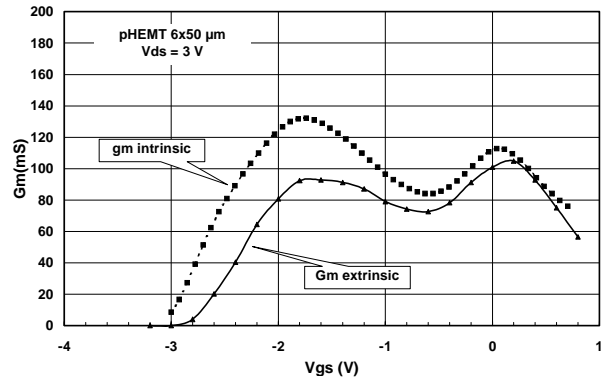


Figure 2 : Evolution of transconductances versus V_{gs} at $V_{ds} = 3 \text{ V}$

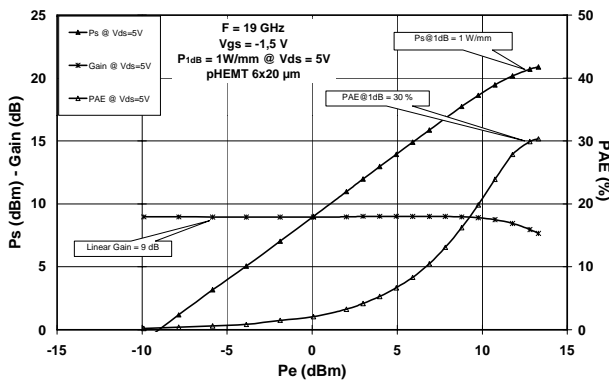


Figure 3 : Single carrier output power, Gain and Power Added Efficiency versus input power for the pHEMT

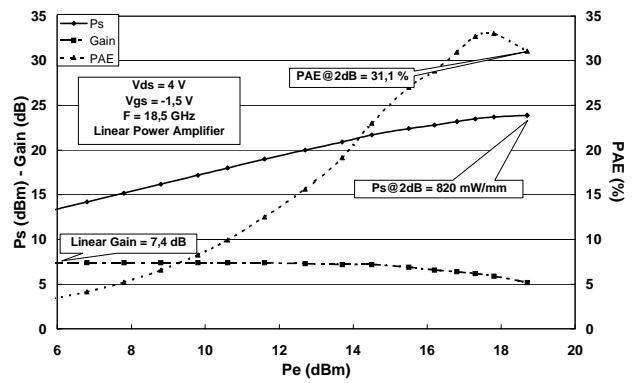


Figure 4 : Single carrier output power, Gain and Power Added Efficiency versus input power for the power amplifier

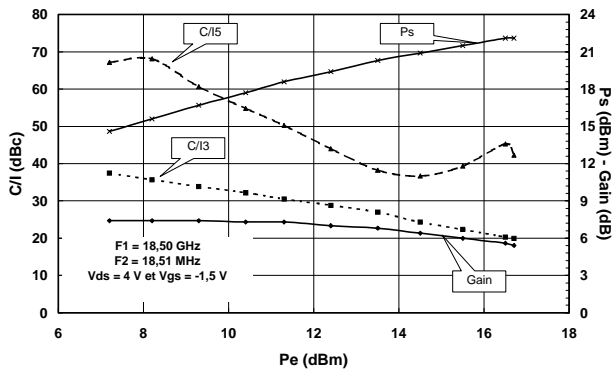


Figure 5 : Two tones intermodulation power response at 18,5 GHz

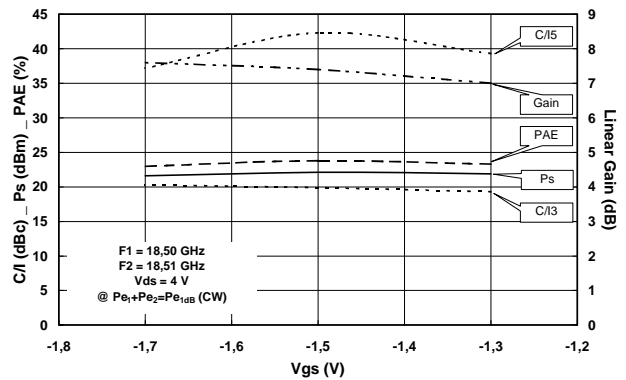


Figure 6 : Evolution of the Gain, Ps, PAE and C/I versus V_{gs} for $Pe_1+Pe_2=Pe_{1dB}$ (CW)

	PHEMT (our study) C/I3	Classical pHEMT C/I3	Classical MESFET C/I3
Ps_{2dB}	19,9 dBc	14 dBc	12 dBc
$Ps_{2dB} - 5 \text{ dB}$	33 dBc	29 dBc	21 dBc
$Ps_{2dB} - 10 \text{ dB}$	42 dBc	43 dBc	40 dBc

Table 1 : Comparison of C/I between different structures