DESIGN AND PERFORMANCE OF GaAs MMIC's FOR L-BAND LOW NOISE FRONT-END APPLICATIONS

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ABSTRACT

This paper describes the design and performance of a GaAs monolithic Low Noise Amplifier and Mixer designed for use in communication systems in the 1.5 - 2.5 GHz frequency band. The low noise amplifier uses a reactive serial feedback configuration and has a measured noise figure of 1.8 dB at room temperature and an associated gain of 20 dB over the full bandwidth. The mixer IC uses an active adder and a FET Mixer, including also an IF output buffer. It provides 9 dB conversion gain without need of external bias networks. This was the first design step towards the integration of the two circuit functions on a single chip.

Keywords: L-Band, Low Noise Amplifier, Mixer, Front-end

1.INTRODUCTION

Recent developments in GaAs material technology and the parallel stabilization of manufacturing processes are resulting in an increasing employement of MMIC as key circuits to reduce costs and to improve performance in telecommunication systems. This paper describes the work we have developed under a concrete application pull for the realization of suitable LNA and MIXER circuits to be integrated in a front-end module for use in point to multipoint digital radio links. After the definition of the final target, the design philosophy was directed to select suitable configurations for each circuit and a consolidated process of 0.8 μm MESFET gate length was chosen to guarantee the specified global performance with low cost, high-yield devices. The good measurement results on the demonstrators after the first processing iteration in the foundry gave us important information and the necessary confidence to integrate the two functions on a single chip. The fabrication of this chip is currently in progress as conclusive part of the front-end design.

2.CIRCUIT DESIGN

The front-end module consists of a low noise amplifier and a FET mixer, and was designed to use a band-pass external filter to reject out-of-band noise (Ref.1,2), as showed in fig.1.

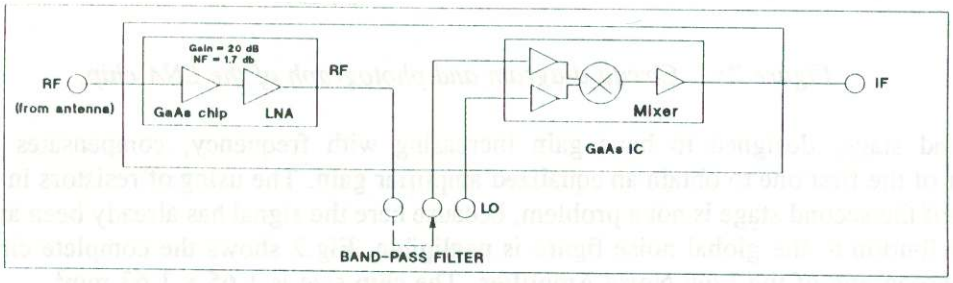

Figure 1: Block diagram of the front end module.

A total gain conversion greater than 15 dB and a noise figure of about 2 dB were required. This meant the design of a very low noise amplifier and of a mixer with positive gain conversion. Circuits were designed using the circuit simulators Touchstone and Libra for linear and non-linear analysis respectively (Ref.7). Measured FET S-parameters and equivalent circuits for passive elements were used, including all parasitic effects. FET non-linear model parameters (Ref.8) were optimized by an in-house software, fitting its DC curves and measured S-parameters at different operation bias points.

2.1.Low Noise Amplifier

Among different circuit topologies for a LNA (Ref.1-3), a lumped LC matching configuration was selected as the most suitable to achieve low noise figure and a high gain with a relatively low power consumption. This parameter, not very severe for our application, was taken into account for save power in the remote units. Two stages of amplification using 600 μm gate width FETs allowed a predicted gain of more than 18 dB and a noise figure of about 1.6 dB (fig.5). Similar performance could be obtained using FETs with larger gate width (900 μm). In the first stage, besides lumped LC elements for impedance matching , inductive series feedback at the source was employed to improve amplifier input VSWR and noise figure (Ref.3). The drawback of reactively matching at L-band frequency is the need of some monolithic spiral inductors with large inductance values. High inductance can be obtained increasing the number of spiral turns, that is the total line length, but degrading the real RF performance for the large influence of the parasitics, as well as the total MMIC size. The value for all the spiral inductors employed in the MMICs was held below 10 nH, so guaranteeing a resonant frequency greater than 5 GHz and consequently the accuracy of the MMIC design in the interest frequency band. The loss of the input matching network adversely affect the amplifier noise figure performance, so that serie parasitic resistance of the inductors had to be minimized in first stage, increasing the spiral line width. As a consequence, bigger size inductors are clearly visible in the first stage matching circuit (see chip photograph in fig.2).

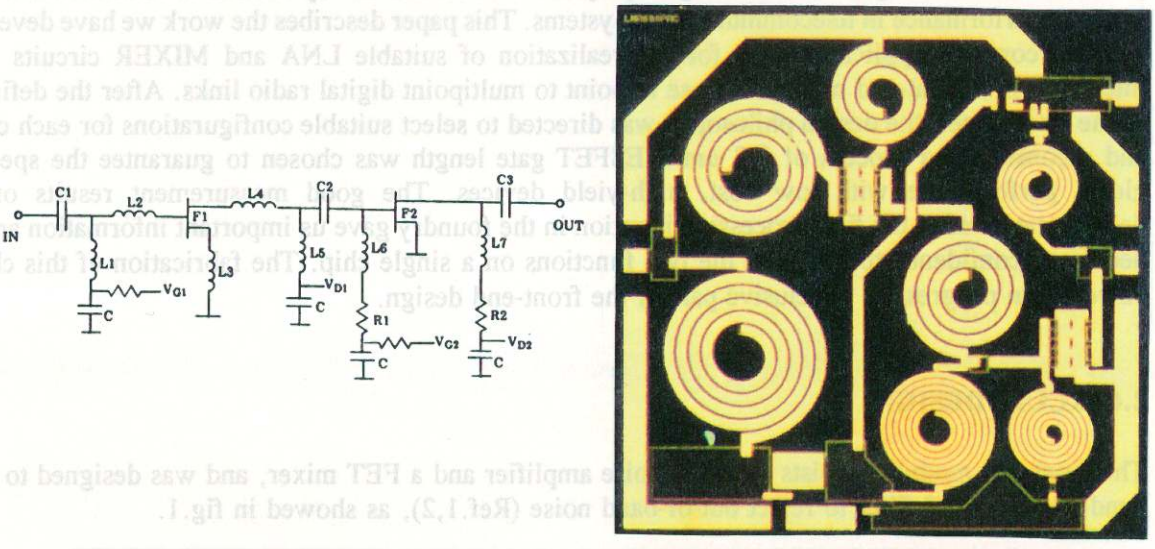

Figure 2: Circuit diagram and photograph of the LNA chip.

The second stage, designed to have gain increasing with frequency, compensates the opposite behaviour of the first one to obtain an equalized amplifier gain. The using of resistors in the matching networks of the second stage is not a problem, because here the signal has already been amplified, and their contribution to the global noise figure is negligible. Fig.2 shows the complete circuit diagram and the photograph of the Low Noise Amplifier. The chip size is 1.65 x 1.63 mm^2.

2.2.Mixer

As mixing element a 0.8 x 600 μm Single-Gate FET was chosen. Its square law characteristic can be applied to frequency conversion. Several configurations are available to supply LO and RF power to the device. We decided to implement a gate FET configuration applying both the RF and LO power across the gate (Ref.4). The large signal LO linearly modulates the trasconductance (g_m) of the device so that, when a small signal RF is applied simultaneously, the drain current is proportional to their product. To get the maximum conversion efficiency, the FET should be biased at the point where the derivative of the transconductance is maximum. This point is close to the pinch-off of the FET. A filter consisting of a capacitor eliminates the sum of frequencies signal, the LO and the RF, so only the frequency difference signal -the IF- remains. An input matching network composed of two inductors grounds any spurious signals or noise at the IF frequency. It is placed at the gate of the mixer FET to match its input impedance with the active adder output and to equalize the conversion gain. The active adder combines the RF and LO signals (Ref.5). It consists of two common-gate drain connected FETs, presenting at their source an input impedance equal to $1/g_m$, where g_m is the transconductance of the FET. Choosing an appropriate gate width and biasing the FET so g_m=20mS, this impedance will be 50 Ω. The active adder, besides giving a good input matching, provides isolation between the RF and the LO ports because of the unilateral behaviour of the transistors. A DC-coupled source-follower output stage is used to amplify the IF signal and as impedance buffer to guarantee an output impedance close to 50 Ω at IF frequency. Fig.3 shows the circuit diagram and a photograph of the device. The chip size is 1.2 x 0.95 mm^2.

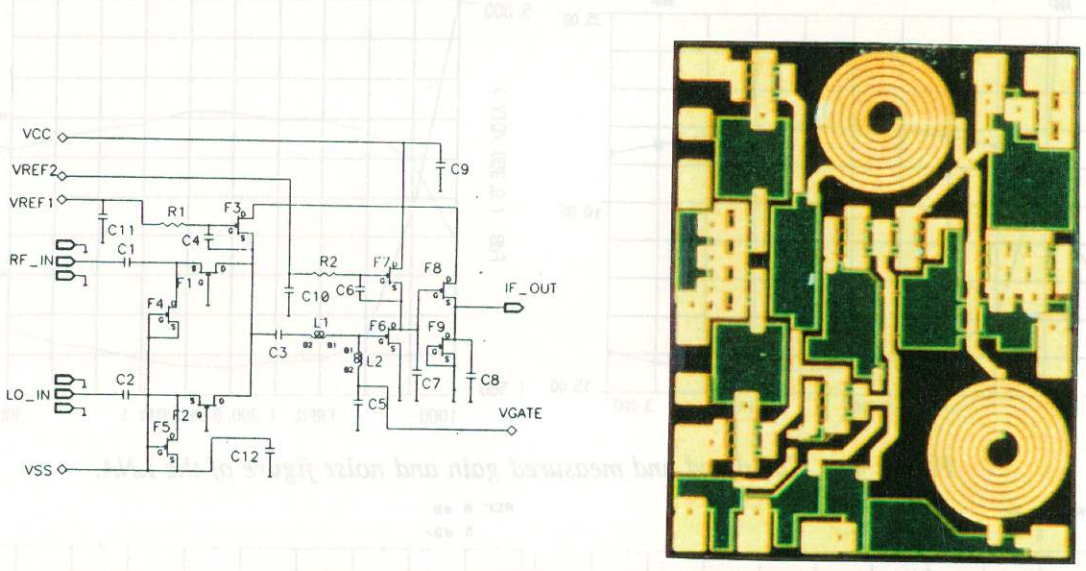

Figure 3: Circuit diagram and photograph of the Mixer chip

2.2.1.Mixer Biasing

In order to achieve a small chip area, a full active bias is used for mixer circuit. The current is injected to the source of common-gate (active adder) and common-drain (buffer) FETs by FETs working as current sources. To avoid the stability problems at DC of the conventional active loads, frequency dependent active loads (Ref.6) have been used for the rest of the circuit. At high frequency, the capacitor between gate and source of the load behaves as a short circuit, so the FET presents R_{ds} as source impedance. At DC, the FET behaves as a source-follower stage and the impedance shown at the source is $1/g_m$, much lower than R_{ds}. This allows to use the network as frequency choke and at the same time to maintain fixed its source DC voltage to the value applied at its gate, without being affected by changes in LO power across the device, or by parameters spread of the process.

3.MMIC FABRICATION

MMICs were fabricated using a funded selfaligned processing technique called DIOM (Double Implantation One Metallization) (Ref.9) with a gate length of 0.8 μm. The use of via-holes was avoided to achieve a better fabrication yield. Airbridge technology was also available for MMIC's layout design. The chips are provided of large ground pads for multiple ground connections.

4.EXPERIMENTAL RESULTS

4.1.Lna Performance

The LNA circuits were characterized on chip with cascade probes and on bench by suitable testing jigs. For cascade measurement the circuits were attached to a metal plate by epoxy resin, the bias being applied to the relevant pads through wire bondings to 100 pF bypass capacitors connected by pointed probes to the bias supply. The test was carried out under different current bias conditions for each amplifier stage to determine the optimum D.C. bias points. A gain of 20 dB and a noise figure below 1.8 dB, a little worse than the predicted one, were achieved. Simulation results and on chip measurements are compared in fig.4. S11 and S22 parameters are showed in fig.5. Similar performance were obtained on bench with the assembled testing jigs.

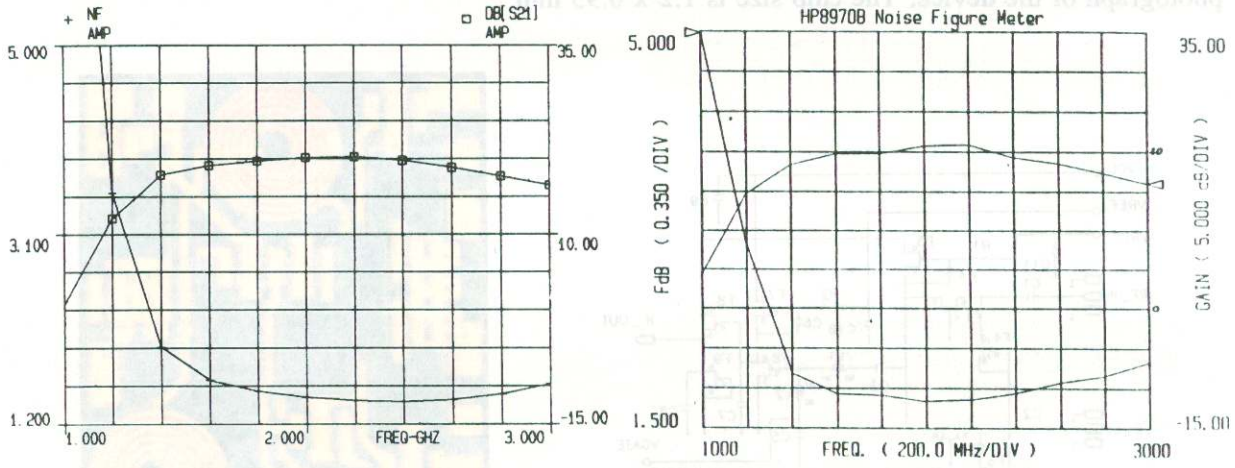

Figure 4: Simulated and measured gain and noise figure of the LNA.

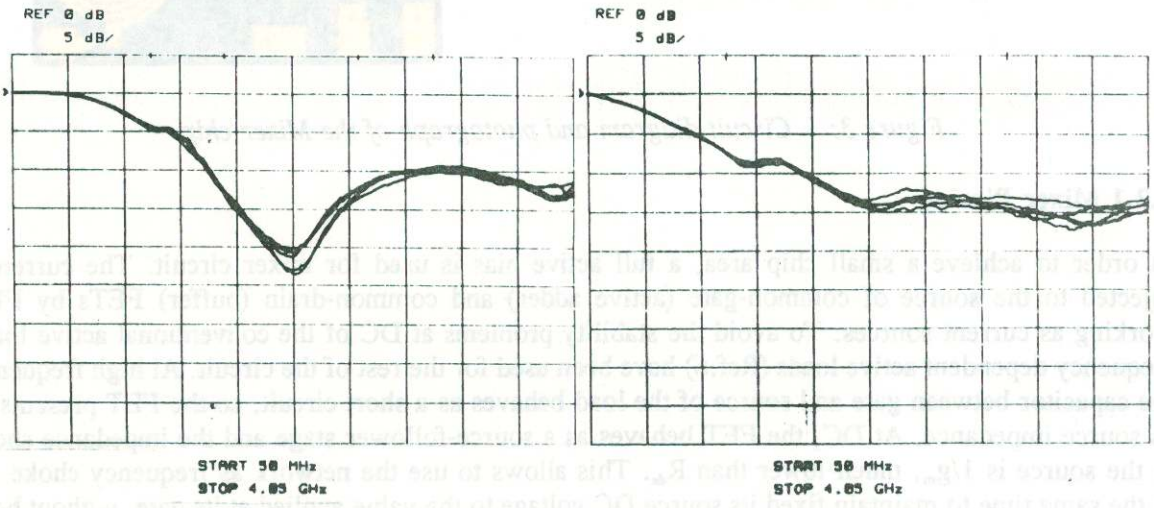

Figure 5: S11 and S22 measured parameters (5 samples).

4.2.Mixer Performance

For the mixer circuit cascade measurement was not possible owing to chip dimensions which required not conventional GSG probeheads and a special needle card for bias supply. The circuit was mounted on a testing jig (fig.6) and tested in the whole RF bandwidth at different IF frequencies (from 30 to 100 MHz). The necessary local oscillator power for maximum efficiency is between -5 and 0 dBm. The input matching at the LO and RF ports is better than -15 dB over the full bandwidth. The output impedance at the IF ports is also close to 50 Ω. The RF to LO isolation is of about 20 dB all over the band, demonstrating the good operation of the active adder (Fig.7). Fig.8 shows the conversion gain and noise figure versus RF frequency compared to simulation for a fixed IF of 70 MHz. The conversion gain decrease at higher IF frequencies due to the RF filter capacitors.

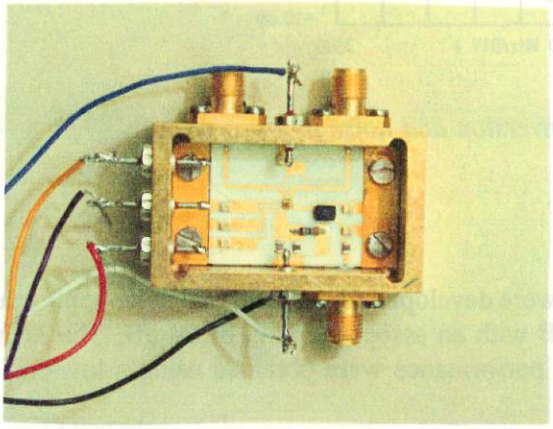

Figure 6: Mixer testing jig photograph

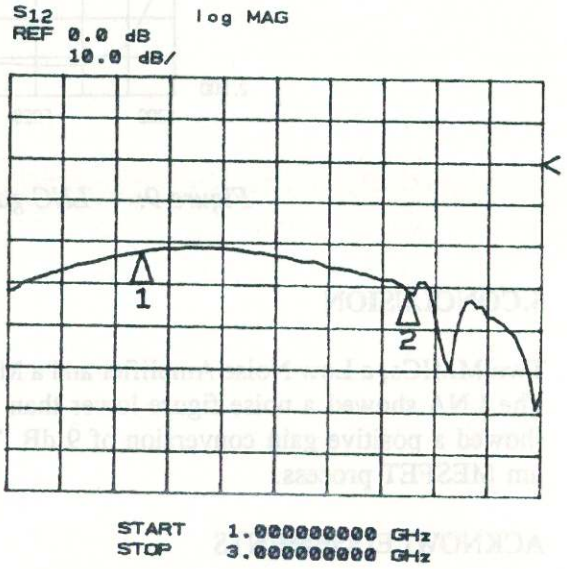

Figure 7: LO to RF isolation measurement

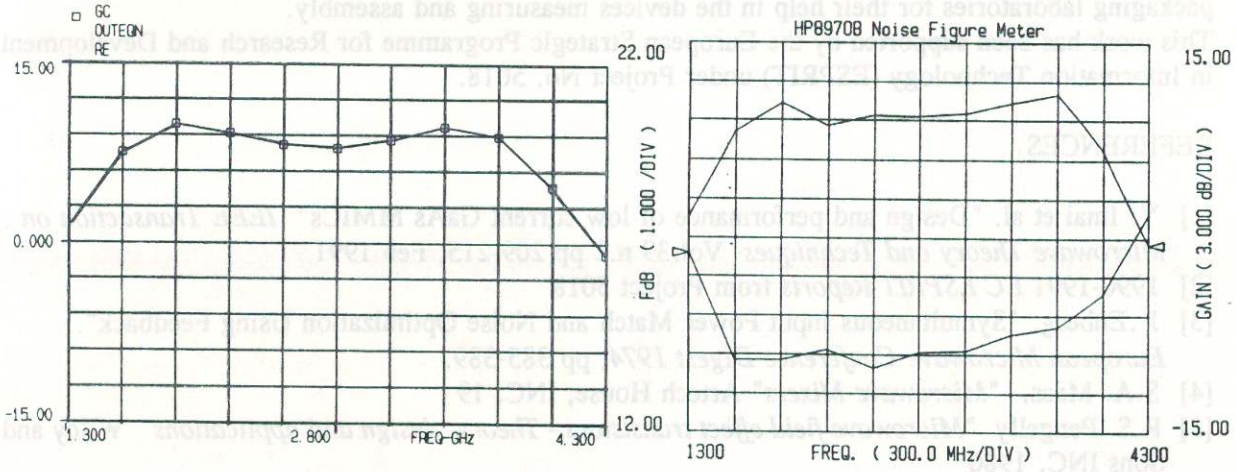

Figure 8: Mixer simulation and measurement comparison

4.3.Low Noise Converter Performance

To evaluate the global performance, measurements of the whole front-end module were carried out connecting in serie LNA and Mixer testing jigs. A total gain conversion of 29 dB an SSB noise figure

of 2.4 dB could be obtained (fig.9).

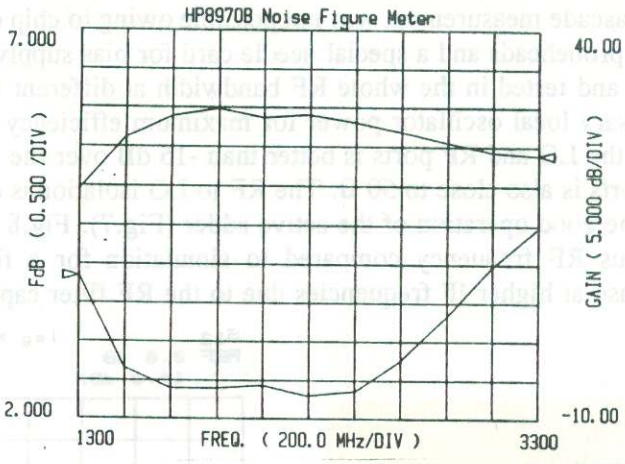

Figure 9: LNC gain conversion and noise figure

5.CONCLUSION

Two MMICs, a Low Noise Amplifier and a Mixer, were developed for L-Band low noise applications. The LNA showed a noise figure lower than 1.8 dB with an associated gain of 20 dB. The MIXER showed a positive gain conversion of 9 dB. These performance were obtained using a low-cost 0.8 μm MESFET process.

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