# Application of Silicon-based RF IC devices in space communication systems & equipment

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***Abstract*—In the next few years, we will see the construction of systems based on constellations of medium size satellites, in which the quantity of equipment to be produced will be very large. The high production volume and compressed lead-time require a technology solution to achieve high integration and repeatability. This paper presents the design and performance of a highly-integrated silicon bipolar RF IC for space applications. The chip offers an Intermediate Frequency Chain, which realises two basic electrical functions: an active mixer and a broadband IF amplifier with an automatic gain control (AGC).**

## I. INTRODUCTION

The satellite telecommunication market demand for new services implies a rapid evolution of the satellite payload configuration and architecture. Basic trends are the communication to and from ground at higher frequencies, increase in the payload capacity, the use of OBP (*On-Board Processing*) and baseband on-board switching network, the need for crosslink communication to relay inter-satellite data. Some payload configurations foresee a direct frequency conversion down to IF frequencies. In this scenario, it is necessary to develop new technologies, in order to build highly reliable, low cost and lightweight equipment, and architectures requiring minimal tuning effort. The high production volume and compressed lead-time require a technology solution to achieve high integration and repeatability. The RF IC technology allows the integration of complex functions, at frequencies less than 1 GHz, like IF amplifier, frequency synthesiser and analog demodulators. The possibility to procure the devices in both ceramic packages and in chip form support the high integration factor achievable with advanced packaging and interconnection techniques like Multi-Chip Module (MCM) and Low Temperature Ceramic Cofiring (LTCC).

The possibility to realise an integrated Intermediate Frequency (IF) strip common to different equipment classes has been identified. The analysis of this main building block highlighted the need of two basic electrical functions: an active mixer and a broadband IF amplifier. Starting from these considerations, a single chip has been designed by Alenia Spazio and realised by a European foundry. The application in space hardware brings a dramatic increase of the integration factor with respect to standard hybrid technology. In fact the two functions are fully independent allowing the maximum flexibility in their use, from the direct connection to the single function utilisation. A complex design technique and the latest CAD tools have been chosen to maximise the advantage of the silicon process used.

## II. CIRCUIT DESIGN AND MEASUREMENT RESULTS

The goal of this project was to design an integrated up/down converter chip to meet the needs in 10 MHz-1Ghz satellite equipment. In order to meet the systems requirements, the amplifier, in differential I/O configuration, should achieve ≥ 45 dB gain, 45 dB linear control gain, output 1 dB compression point ≥ -6 dBm and bandwidth ≥ 800 MHz; the mixer, in single input configuration and differential output, should achieve ≥ 7 dB conversion gain, a RF input bandwidth ≥ 1 GHz, an IF output bandwidth ≥ 800 MHz and port-to-port isolation ≥ 20 dB.

### *A. IF Amplifier*

Fig.1 shows the circuit configuration. It is a three-stage differential amplifier with an output buffer. Each stage has been realised in cascode configuration. This configuration combines the advantages of the common emitter and common base circuits: the low load resistance of the amplifier in common emitter configuration reduces the Miler effect and extends the cutoff frequency, the amplifier in common base configuration doesn't suffer from the Miller effect and doesn't limit the high frequency response. Therefore, it has been possible to achieve very large bandwidth up to 1 GHz with 45 dB gain. Other features have been implemented like a self-compensating bias network (PTAT) for performance stability versus temperature ($\Delta G<1$ dB in the range $-30°\div+70°$), offset control circuitry and finally gain control capability on the full dynamic range [1,2]. The AGC is implemented with a current subtraction system. The advantage is that, under

specific bias conditions, no reduction of bandwidth and no changes in 1 dB compression point are shown. Moreover, the AGC is internally temperature compensated to provide at the same control voltage the same gain in the overall temperature operating range ($\Delta G<1$ dB in the range -30°÷+70°, Fig.4). The performance is summarised in Table I, where the simulations are shown for comparison. Only measured data for packaged amplifier are available at the time this manuscript was prepared. The configuration of amplifier under test is differential at the input and single at the output. Fig.5 shows the amplifier bandwidth. Fig.6 shows the amplifier output level at different control voltage. For each 0.1V of control voltage, the amplifier presents a linear gain variation.

*B. Active Mixer*

Fig.2 shows a simplified circuit schematic. The mixer is a double balanced mixer based on Gilbert cell [3]. It comprises a common base driver stage, a differential switching pair and an open collector output buffer. The common base stage reduces the noise contribution from the switching pair and provides for a 50 ohm input match. The subcircuit responsible for RF makes the voltage to current conversion, transfering the current to the mixer nucleus, which works like a cascode and amplifies the signal coming from the LO ports with opposite phases. The cascode acts like a switch for the RF signal and it is driven by the LO signal phase. The resistive degeneration of differential pair improves the mixer linearity at the expense of a higher noise figure. The LO signal amplitude has been chosen to minimise the noise contribution, in fact a large LO signal reduces the switching duration. The optimum value for this application has been determined equal to 0 dBm. The performance is summarised in Table II, where the simulations are shown for comparison. Only measured data for packaged mixer are available at the time this manuscript was prepared. Fig.8 shows the output spectrum of the mixer for 387 MHz sinusoidal input signal of –40 dBm at RF port and for 337 MHz sinusoidal input signal of 0 dBm at LO port. The configuration of the mixer is single-ended at the input RF and LO port and single-ended at the output

## III. TECHNOLOGY

The die photograph of the IC is shown in fig.3. In fig.7 its use in the engineering model of a frequency down converter for regenerative payload design is shown. The Analog Asic has been designed by Alenia Spazio and manufactured on Thomson-Tcs bipolar process (HSB2), which supports the Polyuse_W family, capable of 5V operation. The Polyuse_W product is a family of pre-diffused arrays made of tiles of uncommitted discrete components: bipolar transistors, resistors, capacitors, inductors and diodes. The design consists in the customisation of the top metallization. Take into account that the chip area is less than 25mm$^2$ the mass and volume reduction is consistent with the full equipment design approach. The fig.9 shows the reduction in terms of mass and power consumption with respect to a traditional approach.

## IV. APPLICATION IN INTEGRATED COMMAND RECEIVER

The speed of digital hardware is continuously increased together with the limit of maximum sampling rate consequently moving the boundary between the analog and digital domain to higher frequency.
The massive use of VLSI technology for space applications, together with the evolution of the digital signal processing techniques, allows defining tuning-less architecture with impressive achievement in terms of mass reduction and unit miniaturization. The RF IC technology allows achieving in the RF domain the same integration factor reached in the digital domain using VLSI CMOS technology. This approach is used in the present R&D efforts to define and design future constellation systems where high performance, flexible equipment will be required in conjunction with high production rate and very low cost. The minimization of production effort implies a tuning-less approach which in the RF, microwave domain is achievable with use of MMIC, RF IC technology while in the DSP area can be obtained with VLSI ASICs integrating Built In Test equipment and diagnostic functions [4]. The architecture foresees the integration of first and second down-conversion stages and the demodulator sections into a pair of RF ICs: one chip integrates the first IF amplification chain with Automatic Gain Control (AGC) while the other realises the downconversion to the second IF, providing a suitable signal level to the A/D converter. For analog receivers (FM Intelsat like modulation format, PM ESA standard) a single RF IC will be used to realise the demodulation section using phase locked loop circuit (Fig.10). Moreover, on deep space transponders and microwave receivers for remote sensing payloads, the demodulation section is an I/Q demodulator that can be realised also by a RF IC.

## V. APPLICATION TO WIDEBAND REGENERATIVE PAYLOAD

In recent years the satellite applications have seen a strong increase in the space hardware demands mainly for commercial communication services like Fixed Service (FSS), Broadcasting Service (BSS), Mobile Service (MSS). The design of radiofrequency, microwave and millimeter wave equipment and electronics has been dramatically modified in order to allow the space companies to compete in the commercial market keeping high performance but at low recurring costs and with short lead-times. Present payload P/L applications, mainly for commercial communication services demand reduction of dimension and weight, lower recurring costs, improved reliability and high performance. The development of multimedia services depends upon the availability of bandwidth for serving a large population of user terminals with a wide range of services. The high increase in the number of channels in both the P/L receiver section (Downconverters) and the P/L transmitter section

(upconverters) has required a strong effort based on the latest qualified technologies that focus on a modular approach. The justification of this R&D effort, is due to the fact that all the down & up converters show the same architecture, based on a double frequency conversion scheme (RF-IF-BB and vice-versa fig.11). The MultiCarrier Demodulators, developed for wideband multimedia satellite are the baseline for a new generation of products that use RF IC technology. This technology makes possible a high integration factor, for miniaturising the equipment and for reducing the payload mass and volume [5].

## VI. CONCLUSIONS

The development of broadband satellite systems will represent a revolution in communication over the next few years. The design and development of RF ICs has been presented. This technology together with advanced interconnection and packaging techniques is the baseline for the present space hardware development for near future wideband satellite communication systems.

## ACKNOWLEDGMENT

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## REFERENCES

[1] R.J. Widlar
"Low voltage techniques"- *IEEE J. Solid State Circuits, vol. SC-13, pp.838-846* , Dec. 1978

[2] Ruud G.H. Eschauzier et al.
"A 100 MHz 100 dB operational amplifier with multipath nested Miller compensation structure"-*IEEE J. Solid State Circuits, , vol. SC-27, pp.1709-1716,* Dec 1992

[3] K.L.Fong, R.G.Meyer
"Monolitic RF Active Mixer design"-*IEEE Trans. Circuits Sys, vol46, pp.231-238,* Mar 1999

[4] M.C.Comparini
"The Alenia Aerospazio perspective in TT&C Technology: from the first S band Coeherent Transponder to the latest digital technology passing trough the commercial satellite applications"- *1st ESA Workshop on Tracking, Telemetry and Command Systems*, Noordwijk, The Netherlands, June 1998*, Invited*

[5] M.C.Comparini, A.Suriani
"Microwave equipment technologies for wideband Ka band satellite communication systems " – *Fifth Ka Band utilization Conference*, Taormina, Italy, October 1999

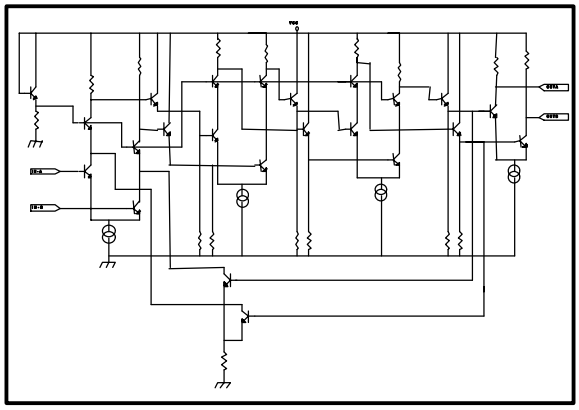

Fig 1:Amplifier Circuit Configuration

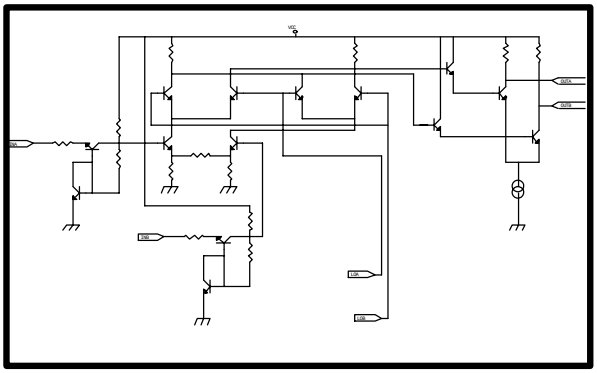

Fig 2: Mixer Circuit Configuration

| Parameter | Simulation | Test |
|---|---|---|
| Gain [dB] | 48 | 45 |
| Noise Figure [dB] | 13 | 13 |
| In 1dB-cp [dBm] | -50 | -50 |
| ΔGain vs T [dB] | 1 | 1.3 |

Table I: Comparison of amplifier performance

| Parameter | Simulation | Test |
|---|---|---|
| Gain [dB] | 8 | 8 |
| In 1dB-cp [dBm] | -13 | -13 |
| ΔGain vs T [dB] | 1 | 2.3 |

Table II: Comparison of mixer performance

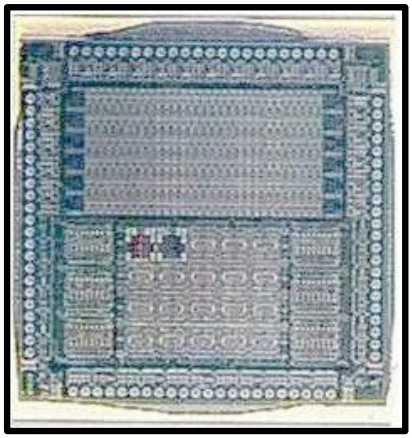

Fig 3: RF IC photograph

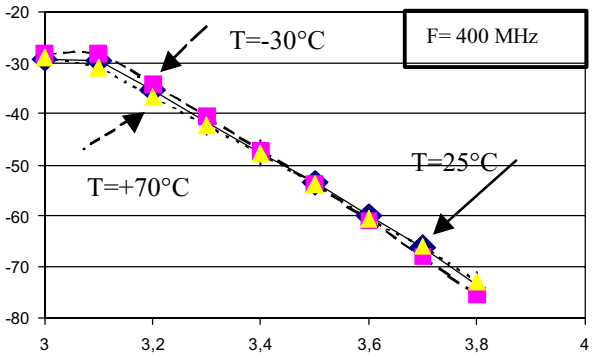


Fig 4: Measured Amplifier Output level vs. Control voltage at different temperatures

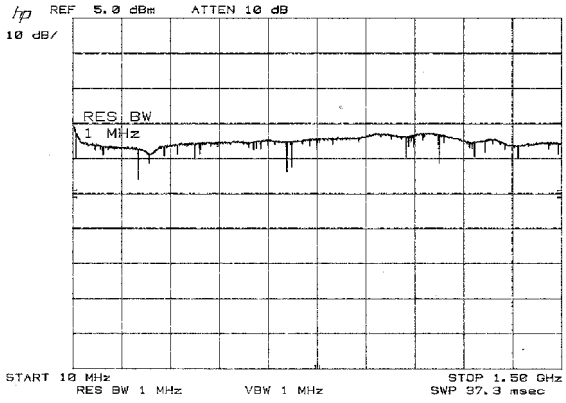


Fig 5: Amplfier Bandwidth

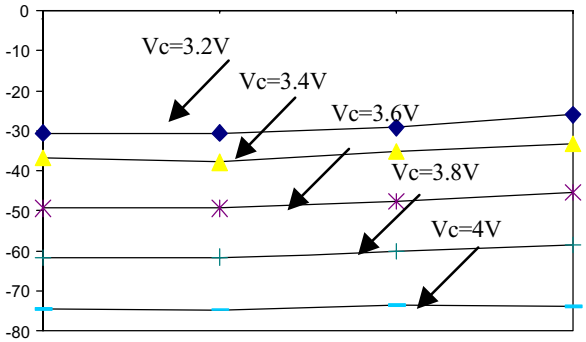


Fig 6: Measured Amplifier Output level vs. Frequency (50MHz-1GHz) for different control voltage level

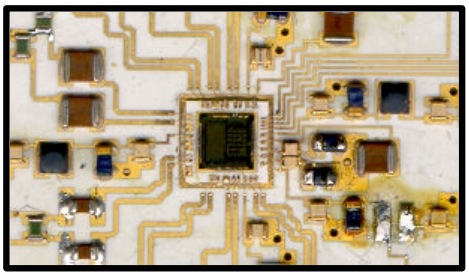

Fig 7: Down Converter Engineering Model

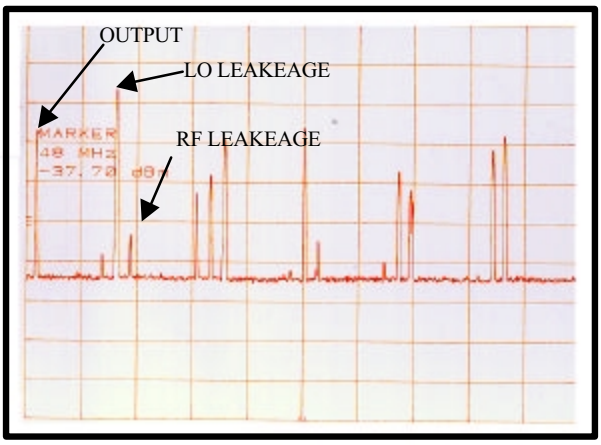


Fig 8: Mixer Output Spectrum ( 10 MHz-2GHz) LO-IF port Isolation 26 dB (LO input level 0 dBm), RF-LO Isolation 23dB (RF input level –40 dBm)

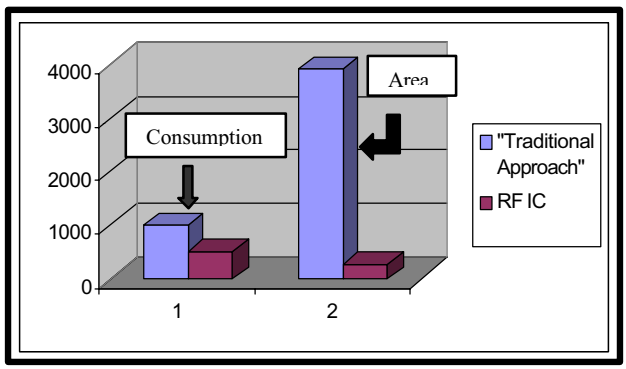


Fig 9: Reduction in terms of power consumption and area respect to the traditional down converter

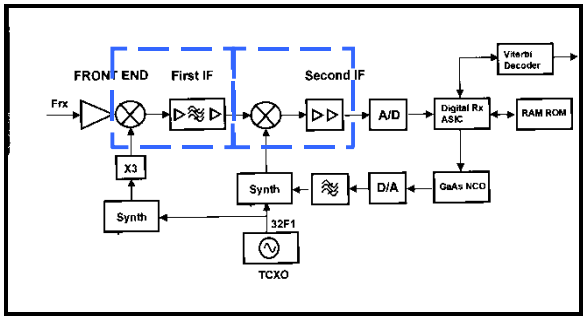


Fig 10: Digital Receiver for Constellation Systems
RF IC Down converter utilization for first and second IF

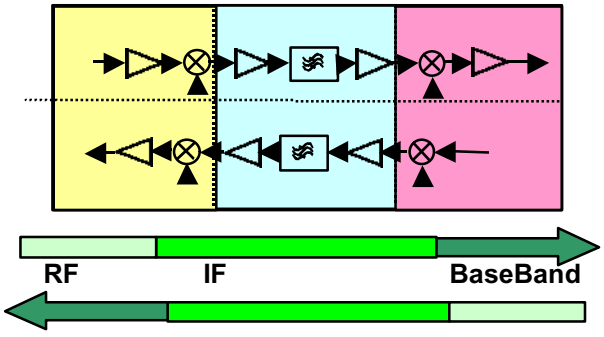


Fig 11: Regenerative Payload Down converter Architecture
RF IC utilisation has been highlighted