Microwave Absorptive MEMS Switches

Guan-Leng Tan and Gabriel M. Rebeiz

The Radiation Laboratory, EECS Department,
The University of Michigan, 1301 Beal Ave., Ann Arbor, MI 48109-2122, USA
Phone: +1-734-936-0183 Fax: +1-734-647-2106
gtan@umich.edu, rebeiz@umich.edu

***Abstract* - This paper describes the design and performance of a 30 GHz CPW SPST absorptive MEMS switch based on silicon surface micromachining technology. The MEMS switch is implemented using capacitive shunt bridges with fixed-fixed beams. A return loss of better than 15 dB and an insertion loss of 0.8-1.0 dB is achieved in the up-state position. The return loss is better than 20 dB and the isolation is 25-30 dB at 30 GHz in the down-state position. Potential application areas include switch matrix communication systems.**

I. INTRODUCTION

Microwave switches have been traditionally designed using PIN diodes [1] or FETs [2]. While these semiconductor switches have very desirable characteristics such as nanosecond switching speed, the power consumption is prohibitively high for emerging applications that demand a large number of switch elements, such as millimeter-wave electronic scanning systems or routing switches in multi-beam antennas. MEMS switches are ideally suited for these applications because of their low power consumption, low cost of fabrication, and excellent electrical performance up to millimeter-wave frequencies.

This paper presents the design and measurement results of a 30 GHz MEMS absorptive switch implemented on high-resistivity silicon substrate. The design is based on capacitive shunt switch elements [3] with thin film tantalum nitride resistors (Fig. 1). Sputtered tantalum nitride is used as it is easy to achieve a 50 Ω/sq sheet resistance, which is suitable for integration in the CPW ground plane. The absorptive switch requires only one extra resistor layer mask compared to a typical reflective switch.

II. DESIGN

Both two- and three-bridge switches are designed. The three-bridge design (Fig. 1) is used when good return loss is required at both ports in the isolation state. The two-bridge design (Fig. 2) is reflective at one port, and is suitable when only one port is required to be absorptive. An additional matching circuit is necessary in the case of the two-bridge switch in order to optimize the return loss in the insertion loss state. This matching network may be placed adjacent to the "reflective" port, as is shown in Fig. 2, but it is also possible to design a more compact switch with a matching network placed between the two bridges.

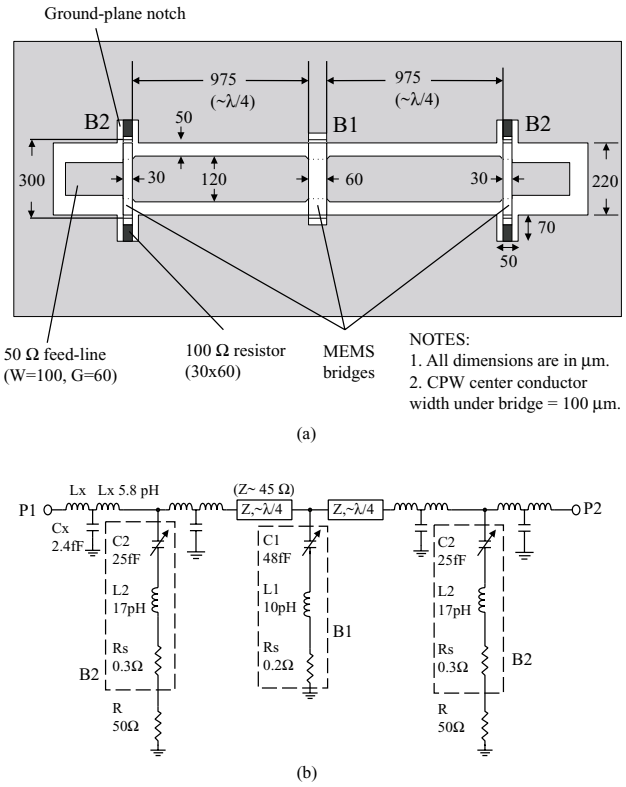

Figure 1: (a) Layout and (b) equivalent circuit of a 3-bridge CPW SPST absorptive switch.

A shunt MEMS bridge can be represented by an equivalent series-LCR circuit [3, 4] (Fig. 1). When the bridges are in the up-state position (insertion loss state), the capacitive coupling to the CPW center con-

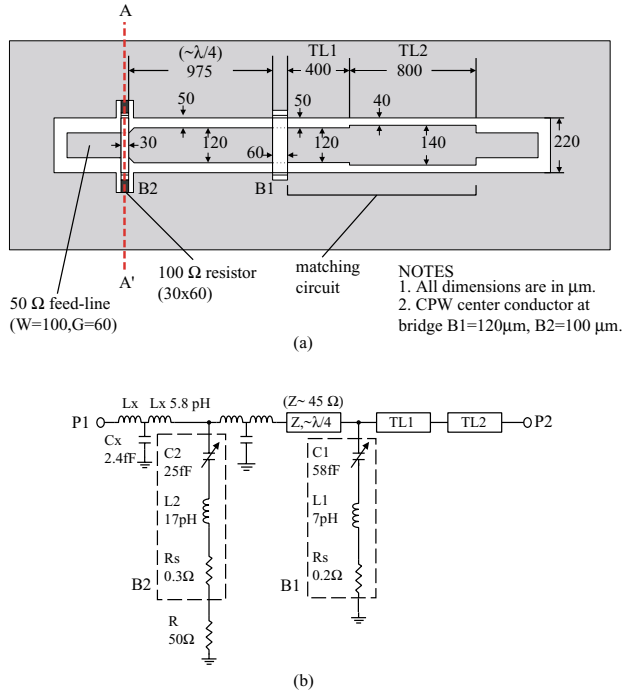

Figure 2: (a) Layout and (b) equivalent circuit of a 2-bridge CPW SPST absorptive switch.

ductor ($C = C_u$) is small and the bridges present only a minor effect on the signal line.

In the down-state position (isolation state), however, the MEMS bridge capacitance ($C = C_d$) increases by a factor of 30-60, presenting a short across the CPW line. The short at the center bridge is transformed into an open at the "resistive" bridges, which are $\lambda/4$ away and are connected to two 100 Ω resistors in parallel. The incident energy is therefore absorbed in the resistors, yielding an excellent match at the design frequency.

The bridge capacitances are estimated using Maxwell 3D [5] software, which determines both the static overlap and fringing capacitances. The inductances of the bridges are scaled from previous characterization [3]. A bridge length of 300 μm and a bridge height of 1.5 μm are chosen to achieve a reasonable pull-down voltage of 15-20 V. For the three-bridge switch, the required up-state capacitance is obtained using a 60 μm bridge ($C_u = 48fF$) for the center MEMS bridge, and two 30 μm bridges ($C_u = 25fF$) for the "resistive" bridges. In the case of the two-bridge switch, the overlap area under the 60 μm bridge is increased to optimize the up-state return loss performance. For both switches, a capacitance ratio ($C_r = C_d/C_u$) of 40:1, or an equivalent C_d of 1.92 pF is obtained using a 1500 Å-thick PECVD silicon nitride layer with $\epsilon_r = 7.6$.

The bridge widths of the the "resistive" bridges are kept to a minimum (30 μm) in order to reduce the losses in the up-state position due to capacitive coupling to the resistors. This is because the insertion loss in an absorptive switch is dominated by losses in the resistors, rather than by reflection and conductor losses. The CPW ground plane notches required for resistor placement are represented in the Libra [6] simulation by series-L, shunt-C T-networks on each side of the bridges (Figs. 1 and 2, Lx = 5.8 pH, Cx = 2.4 fF).

III. FABRICATION

The absorptive switches are fabricated in-house using a five-mask process. A magnified view and the cross section of the switch at the resistor (along A-A' in Fig. 2) is shown in Fig. 3.

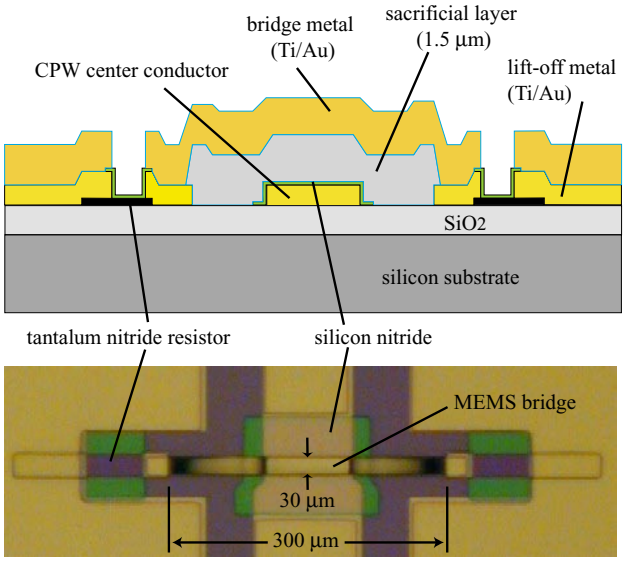

Figure 3: Magnified view and cross-section of the MEMS absorptive switch at the resistor.

High-resistivity silicon substrate ($\rho > 1000$ Ω/cm) with 6600 Å-thick thermally-grown silicon dioxide is used in the switch fabrication. A 700 Å layer of tantalum nitride is first sputtered on the silicon substrate and then patterned using Reactive Ion Etching (RIE) to define the resistors. To prevent non-linear behavior when tantalum nitride comes into direct contact with the gold metallization, a 100 Å W/Ti (90%/10%) layer is sputtered over the tantalum nitride for contact with the gold.

A lift-off process is then used to define the 5000 Å gold metallization for the CPW center conductor and the ground plane. At this point, the W/Ti layer is etched away (except where it comes into contact with the gold metallization), and the resistors are annealed in air at 225 °C to obtain a sheet resistance of 50-55 Ω/sq.

The 1500 Å silicon nitride dielectric over the CPW center conductor is obtained by Plasma-Enhanced Chemical Vapor Deposition (PECVD) at 400 °C, followed by RIE. A 1.5 μm-thick photoresist sacrificial layer is then patterned to define the bridge height. The Ti(500 Å)/Au(1.6 μ) bridge metal layer is blanket-deposited over the entire wafer surface by sputtering, and then wet-etched to define the actual bridge structures. The sputtering also adds another 1.6 μm gold to the CPW conductors. The bridges are then released in a resist-remover and dried using a CO_2 supercritical drying system. The fabricated switches are shown in Fig. 4.

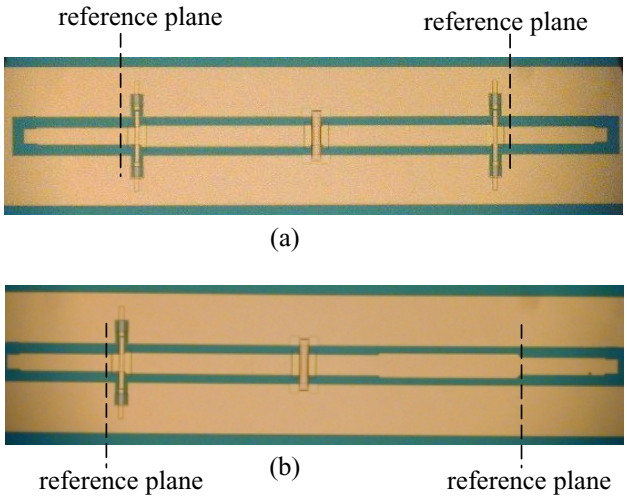

Figure 4: Photographs of the absorptive MEMS switches: (a) 3-bridge design; (b) 2-bridge design.

IV. MEASUREMENT

Measurement of the switches are carried out using a CPW probe station connected to a HP8510C network analyzer. A wideband 2-40 GHz TRL calibration is first performed using the TRL calibration routine "Multical", obtained from NIST. This brings the reference planes to the positions indicated in Fig. 4.

Fig. 5 shows the measured and simulated performance of the three-bridge switch in the up-state position. The insertion loss of the switch is around 0.8-1.0 dB from 24-29 GHz. This is higher than that of reflective switches due to the additional dissipative losses in the resistors. It is possible to improve the insertion loss by using higher or narrower bridges for less up-state capacitance, but this means a higher pull-down voltage. The up-state return loss is better than 15 dB across the same frequency range.

In the down-state position (Fig. 6), a return loss of better than 20 dB is obtained from 24-29 GHz. The 30 dB return loss at 26 GHz corresponds to resistor

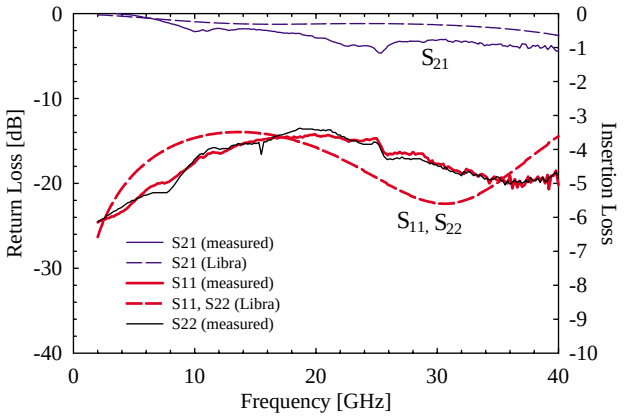

Figure 5: Measured and simulated performance of the 3-bridge absorptive switch in the up-state position.

values of around 53 Ω instead of 50 Ω. Resistors that are exactly 50 Ω will have resulted in a very sharp null in the return loss response, since the $\lambda/4$ line is resonant and presents an "open" at the resistive bridge, and the high down-state capacitance of the resistive bridge effectively shorts the input to the resistors. As the resistor values deviate from 50 Ω, reflection back to the input port increases and the "sharpness" of the null decreases. The return loss bandwidth in the isolation state is restricted by the resonant quarter-wavelength line used to implement the "open" at the resistive bridge. To improve the return loss bandwidth further, it is necessary to employ a circuit topology that achieves a wideband "open", such as a series-shunt approach.

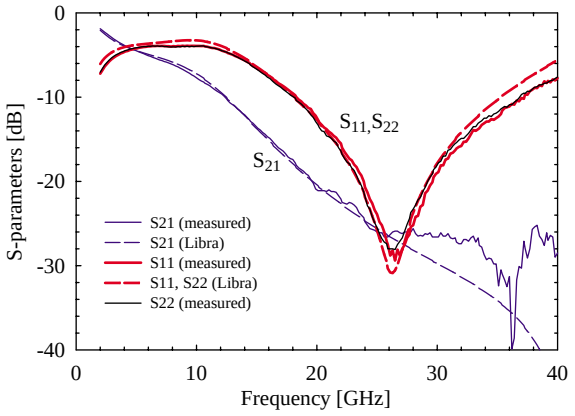

Figure 6: Measured and simulated performance of the 3-bridge absorptive switch in the down-state position.

The measured isolation of the switch is around 25-30 dB, which is lower than the expected value of 40 dB. This is attributed to several issues including the roughness of the nitride underneath the bridge [4], and

stress-related curvature of the bridge in both width and length directions. These fabrication issues result in a lower down-state capacitance as perfect contact between the bridges and the silicon nitride cannot be achieved. When a capacitance ratio of 22 instead of 40 is used in the simulation, the measured and simulated results in the down-state position agree very well (Fig. 6).

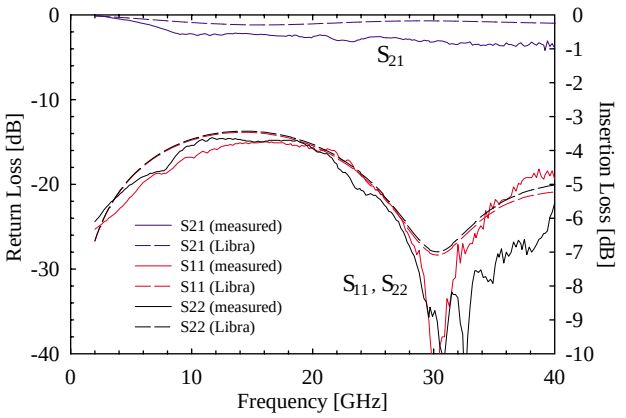

Figure 7: Measured and simulated performance of the 2-bridge absorptive switch in the up-state position.

The measured and simulated results for the two-bridge switch are shown in Figs. 7 and 8. The insertion loss in the up-state position is slightly better as the circuit is shorter. The return loss in the up-state position is better than 18 dB from 22-33 GHz. In the down-state position, port 2 has a return loss of close to 0 dB. This is expected as there is no "resistive" bridge at the output port. Port 1, however, has a return loss of better than 20 dB from 24-31 GHz. The isolation of this switch is around 20 dB at 30 GHz. This corresponds to a model with a capacitance ratio of 18.

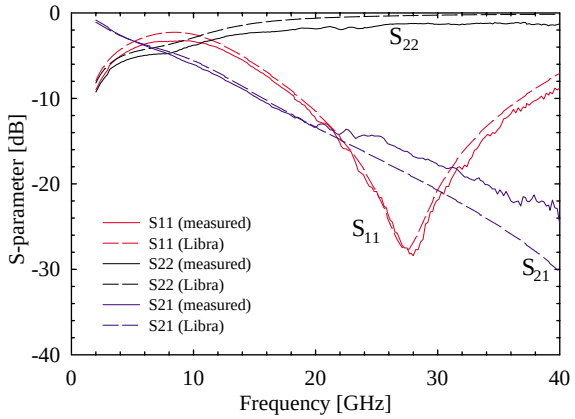

Figure 8: Measured and simulated performance of the 2-bridge absorptive switch in the down-state position.

V. CONCLUSION

Microwave absorptive switches with 0.8-1.0 dB insertion loss and 25-30 dB isolation from 24-29 GHz have been designed using surface micromachining technology. These switches have better than 20 dB return loss in the isolation state. Higher isolation can be obtained by using additional shunt switches, although the achievable isolation may be limited to 40-45 dB due to finite substrate isolation. Good agreement between measured and simulated results is obtained.

References

[1] Alekseev E., Pavlidis D., Ziegler V., Berg M. and Dickmann J., "77 GHz high-isolation coplanar transmit-receive switch using InGaAs/InP PIN diodes," 20th Annual IEEE Gallium Arsenide Integrated Circuit Symposium, 1998, pp. 177-180.

[2] Mizutani H., Funabashi N., Kuzuhara M., Takayama Y., "Compact DC-60-GHz HJFET MMIC switches using ohmic electrode-sharing technology," IEEE Transactions on Microwave Theory and Techniques, vol.46, no.11, Nov. 1998; pp.1597-1603.

[3] N. Scott Barker, Gabriel M. Rebeiz, "Distributed MEMS True-Time Delay Phase Shifters and Wide-Band Switches," IEEE Transactions On Microwave Theory and Techniques, vol.46, No.11, Nov 1998, pp. 1881-1890.

[4] Jeremy B. Muldavin and Gabriel Rebeiz, " High Isolation MEMS Shunt Switches - Part 1: Modeling," IEEE Transactions on Microwave Theory and Techniques, Vol.48, No.6, Jun 2000, pp.1045-1052

[5] Ansoft Maxwell 3D, Release 1.9, 1998.

[6] HP Co., Santa Clara, CA, HP EESof Communications Design Suite v 6.1, 1996.