ORIGINAL TOPOLOGY OF GaAs-PHEMT MIXER

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Abstract : An original topology of GaAs-PHEMT mixer is investigated under high conversion gain consideration. Mixer topology is based on "LO source-injection" concept, since RF, IF and LO signals are respectively applied on the gate, drain and source terminals of the mixing transistor. The conversion matrix formalism allows both the optimization of matching and filtering cells and the assessment of the nonlinear stability. For 14 to 12 GHz frequency conversion, the designed MMIC single balanced mixer exhibits a conversion gain of 5 dB at -15 dBm LO power for a total power consumption of 88 mW and chip size about 0.9 mm^2. The other performances are an output IP3 of 7 dBm for –8 dBm LO Power and a NF of 7 dB.

I. INTRODUCTION

Nowadays, with the development of satellite constellation at low earth orbit (LEO) for example, the GaAs-MMIC market requires reliable low cost solutions in microwave repeaters for Ku band. This leads to the multifunction concept [1], which consists in including several "building blocks" (amplifier, power splitter, power combiner and mixer) on the same GaAs chip. This concept may first improve performances of system in reducing parasitics and mismatches of interfaces between blocks , and secondly reduce design time and cost with the availability of a generic library of optimized circuits.

The functional study of these multifunctions shows that the mixer conversion gain plays a central part in the overall global performances of the system. With sufficient mixer conversion gain, the total number of amplifiers is actually minimized as well as the power consumption and the chip area, while noise and linearity are governed by first stage and last stage respectively. This resulting decoupling of frequency conversion system performances is well suited for optimization and makes the design easier.

In this paper, we report on an original active mixer which both presents a high conversion gain and a structure well suited for its integration in a double balanced design. Section II presents the topology of the mixer, the mixing process and the function of each element. Section III addresses the design methodology based on conversion matrix theory. A special care is focused on the nonlinear stability. The validation of these concepts are made in section IV. In the last section, we finally present the designed MMIC and the simulated results which are in accordance with the theoretical potentialities of this mixer topology.

II. DESIGN DESCRIPTION

We focus on a FET mixer which presents a conversion gain as large as possible. In such a case, the main operated nonlinearity must be the transconductance of the FET : the RF signal is applied on the gate and the IF one is retrieved on the drain. The most simple way to inject the LO signal to pump the transconductance is to put it on the last unused pin : the source [2]. This is realized with the adjunction of a transistor, which moreover minimizes LO power. This principle leads to the mixer configuration in black continuous line of Figure 1.

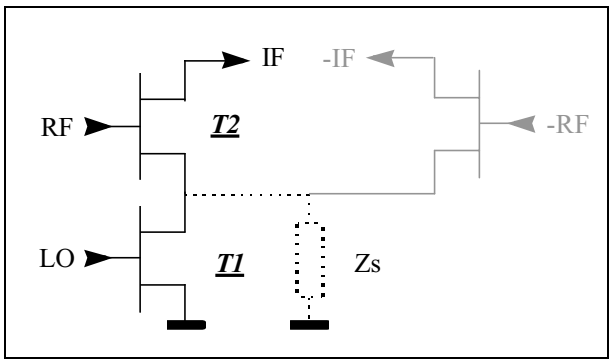

Figure 1 : Topology of the mixer

Figure 2 presents the transconductance variations of the transistor T2 versus voltages V_{LO} and V_{RF} applied on LO and RF accesses respectively. As it can be seen, if the voltage V_{LO} is large enough, the transistor T2 transconductance Gm is time varying at LO frequency. On this graph, the thick line shows the optimal pumped cycle in which the variation of Gm is maximal. This demonstrates conversion mechanism and realizes a support for the choice of transistors quiescent points.

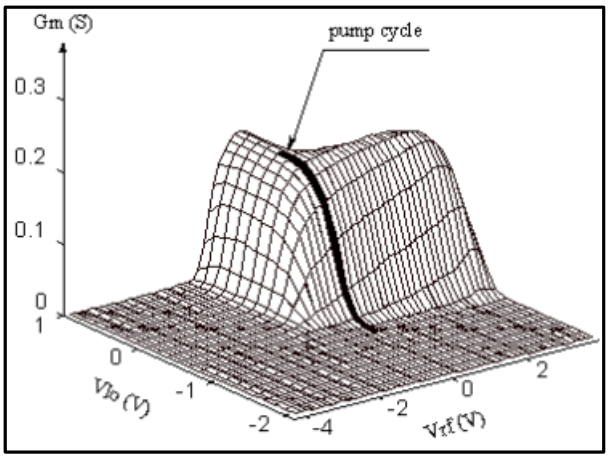

Figure 2 : Transconductance of T2 vs Vlo and Vrf

The optimal conversion gain is then achieved when transistor T2 remains in its saturation region throughout the LO cycle. Consequently the transistor T1 operates in its linear region. Conversion gain of this topology has the same analytic expression as the gate mixer one [3] and is maximized when mixing transistor has 6 gate-fingers with 50 µm width. The transistor T1 dimensions have to be sufficient to modulate drain-source current of T2 from zero to Idss (which corresponds to the maximum variation of the transconductance).

While the principle of operation is relatively simple, load precautions may be considered for each access. First, the efficient pump of the transconductance of the transistor T2 needs a low impedance load at LO frequency for the two RF and IF terminals. Secondly, as we will present in the next section of this paper, an impedance Zs has to be added on the source of the transistor T2 (in dotted line on Figure 1) to prevent nonlinear instabilities.

Finally, a single balanced mixer is simply obtained by arranging symmetrically the transistor T2 (in grey on Figure 1).

The next section will focus on the design methodology that leads to an optimum operation of this topology.

III. DESIGN METHODOLOGY

As described in section II, the optimization of loading impedances at RF, LO and IF terminals must maximize the conversion gain and must ensure the stability of the circuit. This optimization is achieved using the conversion matrix formalism, which is well suited to investigate mixers where large and small signals coexist with [3]. First, the circuit needs to be analyzed under only LO large signal excitation. The elements of the transistor's equivalent circuit are then time varying in proportion to the LO pulsation (as depicted on Figure 2 for Gm of T2) and can be expanded in Fourier series. The ohmic equations can be re-written in the matrix form, for example : $\overrightarrow{Id} = \overline{\overline{Gm}} \bullet \overrightarrow{Vgs}$, where $\overrightarrow{Id}$ and $\overrightarrow{Vgs}$ are vectors built with the spectral components of id and vgs for the $f_{RF} \pm k.f_{LO}$ frequencies, and $\overline{\overline{Gm}}$ is a square matrix formed with the Fourier coefficients calculated previously.

Both linear and nonlinear elements of the transistor's equivalent circuit are then converted into a matrix form. A linear representation of the structure is so obtain and popular methodologies for linear circuits can be used to investigate conversion performances. The resulting electrical representation is shown on figure 3 in which Zg (Zl) includes matching, filtering and source (load) impedances.

The conversion gain and rejections are then calculated using the admittance conversion matrix ($\overline{\overline{Ycv(p)}}$) expressed between port 1 and port2 which are respectively connected to a current source at f_{RF} frequency and left open [4].

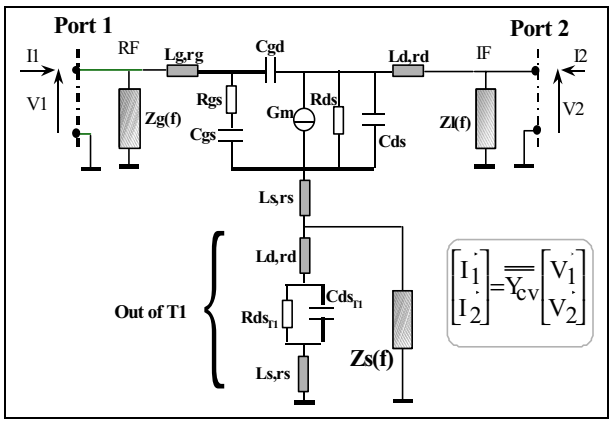

Figure 3 : Electrical modeling of the structure

The optimal matching circuit at RF terminal is then extracted. Thus, we optimize the filter circuit on the IF terminal which must present a matched impedance at the IF frequency and a low impedance value at the RF one (Figure 4). The second condition minimizes the RF frequency contribution on output voltage and prevents any feedback caused by the gate-drain capacitance Cgd of transistor T2 (which may decrease the conversion gain down to 3 dB).

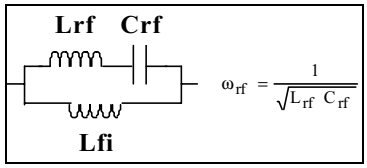

Figure 4 : Circuit at IF terminal.

Moreover, conversion matrices allow the investigation of the nonlinear stability of the circuit which is the key point of this topology. The method we use is based on the return difference concept, primarily introduced by Bode [5], which is a representative function of the natural frequency of the system. In our case this function is expressed as followed:

$$F(p) = \frac{\left|\overline{\overline{Ycv(p)}}\right|}{\left|\overline{\overline{Ycv(p)}}\right|_{Gm=0}}$$

Where $\left|\overline{\overline{Ycv(p)}}\right|$ is the determinant of the admittance conversion matrix previously defined and $\left|\overline{\overline{Ycv(p)}}_{Gm=0}\right|$ is the same determinant when dependant current sources (here Gm) are set equal to zero.

Stability is ensured when no zero of F(p) is situated in the right half plane. According to the Nyquist criterion, this condition is satisfied when F(p=jω) does not encircle the origin critical point when ω varies from 0 to infinity.

Based on previously presented developments, we investigate the nonlinear stability of the circuit and optimize the transistor T2 source to ground impedance Zs in order to insure inconditionnal stability. Figure 5 shows the results of this investigation.

Without the impedance Zs, the Nyquist locus encircles the origin and leads to an unstable behavior. Indeed, the drain-source impedance exhibited by the transistor T1 is capacitive and it is well known that such configuration can be unstable.

To solve this problem, the optimum impedance Zs must exhibit a low impedance value at RF and IF frequencies to prevent instable loop which could take place in the mixing transistor. Such a load may be simply realized associating an inductor Ls and a capacitor Cs in series (top of the figure 5), assuming a resonant frequency near from f_{RF} and f_{IF}. As the resulting Nyquist locus (figure 5) does not encircle the critical point, a stable behavior of the circuit is obtained.

Finally, the values of inductance Ls and capacitance Cs are refined to move away the Nyquist locus from the critical point as far as possible.

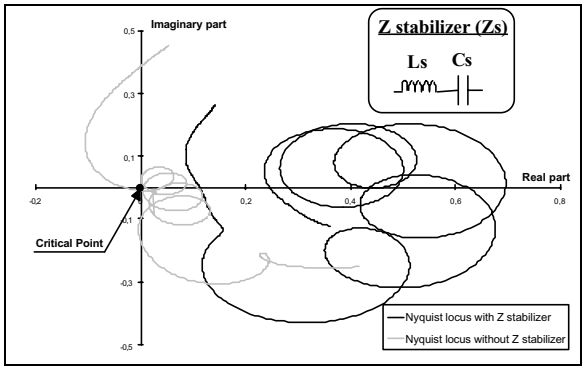

Figure 5 : Nyquist locus, impact of Z stabilizer.

IV. VALIDATION OF THE TOPOLOGY

The complete circuit (figure 6) has been electrically simulated by HP-MDS with matching and filter cells previously calculated using conversion matrices. In this section, passives elements are considered ideals. The Figure 7 shows the conversion gain versus the RF frequency at -15 dBm LO power. The values given by the conversion matrix method are close to Harmonic Balance simulation results overall values of RF frequencies. This validates the conversion matrix theory used to optimized the circuit, especially about the stability. The performances for -15 dbm LO power are : a conversion gain better than 10 dB for central frequency and greater than 0 dB over a frequency bandwidth of 2 GHz, a third order output IM intercept point of 10 dBm and a noise Figure of 3 dB.

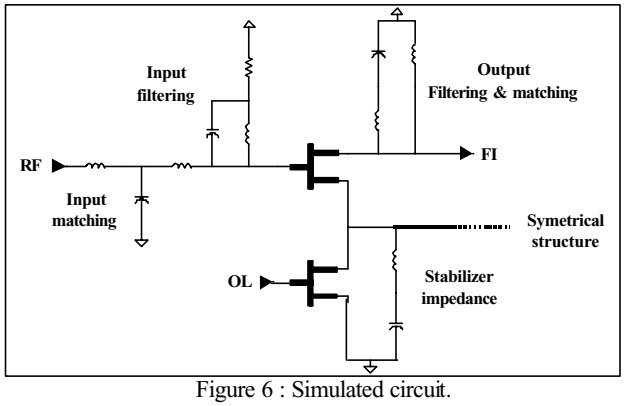

Figure 6 : Simulated circuit.

These results show that this structure presents a conversion gain 6 dB greater than more classical topologies, which consist in inverting the LO and RF signals [6,7].

To summarize, the mixing structure we present in this paper combines the high conversion gain advantage of the gate mixer and the simplicity of classical dual gate mixers, especially about the injections of RF and LO signals.

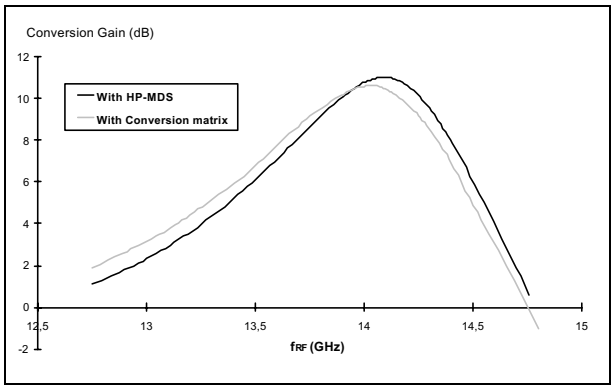

Figure 7 : Simulated conversion gain.

V. MONOLITIC INTEGRATION and RESULTS

The monolithic integration has been made with the Philips Microwave Limeil foundry 0.2µm gate length PHEMT process.

To minimize the MMIC surface, we had to reduce the IF filter inductance dimensions and then the quality coefficient has decreased. The conversion gain is then reduced to 5 dB for –15 dBm LO power (figure 8) but its flatness versus LO power in the range –20/+5 dBm could be an actual benefit. It should be emphasized that this gain is greater than 0 dB over 1.2 GHz bandwidth (figure 9).

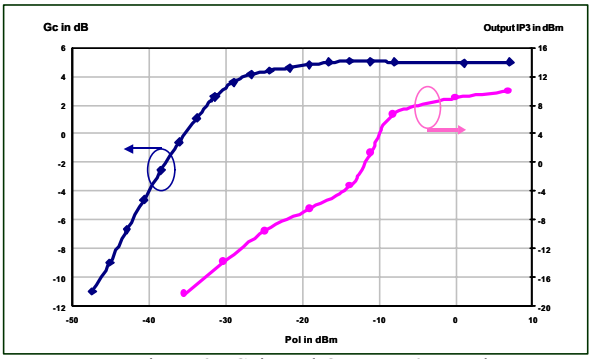

Figure 8 : Gain and Output IP3 vs Pol

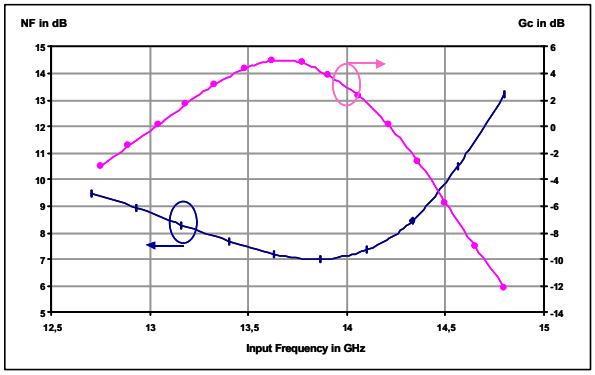

Figure 9 : Gain and NF vs frf

Others performances (figure 8 and 9) are : an output IP3 of 7 dBm for –8 dBm LO power and a noise figure of 7 dB for an input frequency of 13.7 GHz. The low power consumption of this circuit must be noticed : a value of 88 mW is actually obtained.

The circuit is presented on figure 10. Its overall size is about 0.9 mm^2.

Comparing these features with those published for classical dual gate mixer [8] (for same chip size), the performances enhancements are :

+1.5 dB on Gc for a LO power decrease of 18 dB.

-4 dB on NF and +4.5 dB to +8 dB on Output IP3.

-30 mW on power consumption.

The proposed topology is so a good applicant for an optimal integration in a global frequency conversion system, because, as explain in the introduction, its performances are sufficient to transfer constraints of noise and linearity on the first and the last stage, respectively (as illustrated in table 1).

Table 1 : Global Conversion Chain

	Gain (dB)	NF (dB)	OutIP3 (dBm)
First Stage	10	4	-
Mixer Stage	5	7	7
Last Stage	10	-	20
Global Circuit	25	4.6	15

First stage correspond to an active power divider of RF signals to supply the mixer with +RF and –RF. The last one correspond to an active power combiner of +FI and –FI signals delivered by the mixer.

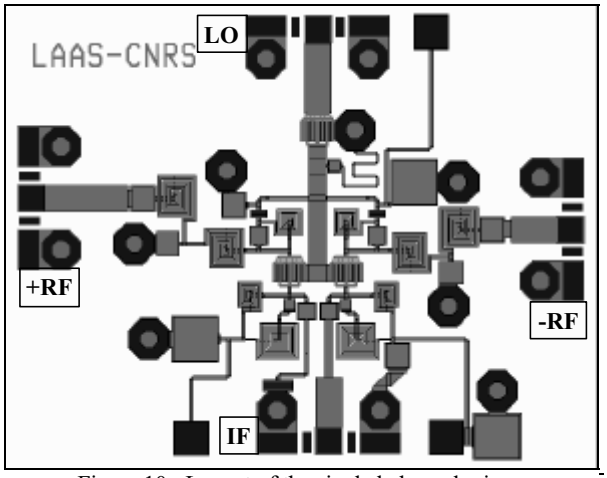

Figure 10 : Layout of the single balanced mixer.

VI. CONCLUSIONS

An original topology of GaAs-PHEMT Mixer has been investigated. The nonlinear stability obstacle of this structure was overcome using conversion matrices. These theoreticals investigations demonstrated the need of a mixing transistor source to ground impedance Zs to assure an unconditional stability. The design and the optimization of the mixer loading circuits have been conducted with this same formalism and were validated by Harmonic Balance simulations.

An MMIC demonstrator of this topology has been designed and is under process. Compared with classical dual gate mixer, enhanced performances are achieved. This single balanced mixer MMIC exhibits a conversion gain Gc = 5 dB at -15 dBm LO power independent of the LO power value, an output IP3 = 7 dB for –8 dBm LO power, a NF = 7 dB and a consumption power of 88 mW on only 0.9 mm^2.

We are now integrating this optimal topology into a frequency conversion global system under both low power consumption and high density considerations.

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