Measurement and Modelling of MIC Components Using Conductive Lithographic Films

P. R. Shepherd *, & C. Taylor *, P. S. A. Evans •, & D. J. Harrison •

*Dept. Electronic & Elec. Eng., University of Bath,
Claverton Down, Bath, BA2 7AY, U.K. Email: P.R.Shepherd@bath.ac.uk
• Dept. of Design, Brunel University,
Englefield Green, Egham, TW20 0JZ, U.K. Email: Peter.Evans@brunel.ac.uk

July 11, 2001

ABSTRACT

Conductive Lithographic Films (CLFs) have previously demonstrated useful properties in printed microwave circuits, combining low cost with high speed of manufacture. In this paper we examine the formation of various passive components via the CLF process, which enables further integration of printed microwave integrated circuits. The printed components include vias, resistors and overlay capacitors, and offer viable alternatives to traditional manufacturing processes for Microwave Integrated Circuits (MICs). Manufacturing data, measurements on test structures and equivalent circuit modelling for a range of CLF circuit structures are presented.

INTRODUCTION

Conductive lithographic films (CLFs) are an emerging fabrication process for microwave circuits and systems. CLF conductors are fabricated on flexible substrates e.g. paper or thin plastic films, using silver-loaded inks and standard offset lithographic printing machines [l]. Offset lithography is the technology used to mass produce books and magazines and is quite dissimilar from the “photo-lithography” processes employed in integrated circuit and conventional MIC production. CLFs were developed primarily as alternatives to traditional etched copper laminate circuit boards for low frequency applications, but have useful properties as substitutes for MIC substrates. It has been previously demonstrated that although losses in CLF circuits are slightly higher than in traditional MIC substrates, there are significant advantages in their use at microwave frequencies. Microstrip structures fabricated via the CLF process including through lines, coupled lines, steps-in-width, and ring-resonators have been produced and measured [2], [3], [4]. Co-planar waveguides and patch antennas have also been constructed. The use of CLF conductors in MICs or other planar structures has two main advantages. Firstly, due to the simple printing process, it provides a cheaper and faster manufacturing process for bulk applications. Secondly, CLF substrates are flexible, and can be readily deformed or bonded to curved surfaces, whereby S-dimensional circuits are achieved. Similar structures are difficult or impossible to achieve via the standard MIC process. In this work, Brunel University - who developed the CLF process - have provided various inks and access to lithographic printing and production facilities. The University of Bath have supplied microwave design, measurement and modelling capabilities.

MICROWAVE TEST STRUCTURES

VIAS

When integrating active components into MICs, it is often necessary to form vias making electrical connections between striplines and the ground plane on the other side of the substrate. In conventional

MIC processes, through-hole-plating techniques are widely employed for this purpose. However, in entirely printed CLF substrates an alternative via manufacturing technology is necessary. Three possible printed-via techniques were therefore investigated. In each case small holes were drilled in the CLF substrates at points where a via was required. To form the electrical connection, the hole was subsequently filled with i) the same electricalIy conducting ink used for the CLF conductors, ii) a proprietary silver-loaded paint iii) a proprietary silver-loaded epoxy resin adhesive. Manufacturing complexity was similar in each case, and the main purpose in evaluating different solutions was to evaluate best the various types of via in terms of their microwave performance. A series of 50 Ω microstrip lines were therefore printed via the CLF process, each being terminated in one of the via structures. The l-port S-parameter of each structure was measured in the range 50MHz - 20 GHz using au HP 8510B vector network analyser (VNA). These measured results were then used to optimise the equivalent circuit, depicted in Figure la. As the VNA was calibrated in co-ax, the reference plane was situated at the start of the SMA to microstrip launcher, hence a model for the launcher and the launch resistance is included in the overall equivalent circuit. The via model consists of a resistance and inductance in series, along with a shunt capacitance. This circuit provided a good optimisation solution (using Ansoft's Serenade software) to provide agreement between measured and the modelled results. The resulting equivalent circuit parameters for the three via structures are presented in Table 1.

We conclude from these results that the best overall solution is the CLF ink via. The other via structures have significantly higher equivalent circuit resistance values. The epoxy via does however possess a significantly lower parasitic capacitance.

RESISTORS

In addition to silver-loaded inks, carbon-based inks have also been developed to realise printed resistor structures. However, printed carbon-based ink films have a relatively high sheet resistivity and relatively low tolerance, and are not at present considered suitable for printing low-value resistors in CLF MICs. The natural sheet resistivity of CLF conductors is approximately 0.l5Ω/ , and this can be increased in a controlled manner by reducing the quantity of ink deposited during printing operations. In has proven possible to produce resistor structures embedded within microstrip lines, by a system of overprinting a gap in a microstrip conductor with a "sparse" printing "pass" of the normal silver loaded ink formulation. Ink films deposited in this manner provide a 3 *m*m thick line with a measured D.C. sheet resistivity of approximately 10 Ω/ .

A nominal 30 Ω resistor was formed in a microstrip circuit, based on this sheet resistivity, and the structure had a measured resistance of 33 Ω at D.C. However, when this structure was evaluated at microwave frequencies, some difficulty was experienced in obtaining a consistent electrical equivalent circuit. This was partly due to the modelling software not being able to optimise the resistivity of the microstrip line as a separate parameter, and the best match that could be obtained in comparison of modelled and measured results was an equivalent resistance of 12 Ω.

This result is significantly different from the measured D.C. value. One reason for this discrepancy is the possibility of a different conduction mechanism in sparsely printed CLF film resistors at high frequencies. Research directed to understanding this anomaly is currently in progress.

CAPACITORS

Further ink formulations have been developed at Brunel which allows printing of dielectric ink films via offset lithography. It was envisaged that overlay (parallel plate) capacitor structures could be embedded within microwave striplines, by overprinting a conductive ink layer with a dielectric film, and finally with another conductive ink layer. The practical problems have included producing ink films of adequate dielectric strength that can withstand the elevated electric field concentrations surrounding the silver flake particulate in the conductive ink. This problem is compounded by the

flake silver possessing similar mean particle size to the thickness of the printed dielectric layers.

A system of overprinting the dielectric layer to increase its thickness and dielectric strength was investigated. This led to sufficiently stable structures in terms of breakdown voltage. However particular attention must be accorded to the thicker dielectric films when printing the top electrode layer, to ensure that the ink film forming the top plate of the capacitor is bonded to the continuing microstrip line. One sufficiently robust capacitor structure was produced by this technique for measurement and modelling purposes.

The printed capacitor model is shown in Figure lb, with the CLF capacitor structure modelled with a series inductor and capacitor, with parasitic capacitances to ground. After optimisation to the measured S-parameters for the system, the following equivalent circuit values were obtained: C_C = 2.6 pF, L_C = 456 pH, C_{E1} = C_{E2} = 0.22 pF. The dimensions of the CLF capacitor were l.0mm x 0.6mm.

Due to the frailty of this structure, an alternative method of constructing overlay capacitors was investigated. This consisted of using a thin (approximately 75 μm) plastic lamination layer between the two CLF metallisation layers. Although this complicates the manufacturing process, requiring removal of the lamination layer in order to contact the lower metallisation, it provides an extremely robust structure, with no problems of dielectric breakdown. A number of different sized capacitors were constructed, measured and modelled, using the same equivalent circuit as that shown in Figure lb. A summary of the equivalent circuit values is shown in Table 2. The results appear to be consistent, with increasing primary capacitance almost directly proportional to the area. The only slight discrepancy is in the parasitic inductance value for the 4 mm^2 device being higher than expected from the trend.

DISCUSSION AND CONCLUSIONS

A novel series of passive components for use in MICs based on the CLF process have been constructed and evaluated.

The via structures between the microstrip line and ground plane have been constructed using three alternative conductive fillings. From the equivalent circuits, it appears that the CLF ink filled via gave the best overall performance.

Resistors based on thinner than normal CLF layers gave consistent results at D.C., but microwave modelling appears to indicate a much lower equivalent resistance. The reasons for this are still under investigation, but this behaviour would not preclude their use in circuits where the DC. resistance is critical, e.g. bias circuits. Resistor structures using improved carbon loaded inks are also under investigation.

Planar capacitor structures using dielectric inks have also been investigated. The necessity to have several dielectric ink overprints, to improve the dielectric strength of the structure, results in a less robust structure. An alternative construction approach for CLF capacitors has been investigated which involves the use of a lamination layer in place of the printed dielectric. This results in a much more robust structure at the cost of some complexity in manufacture. The modelling of different sized capacitors has provided a good consistency of equivalent circuit values.

References

[l] D. Harrison, E. Billett & J. Billingsley. “Novel Circuit Fabrication Techniques for Reduced Environmental Impact” International Conference on Clean Electronic Products and Technology, Edinburgh, UK, 9th - 11th October 1995.

[2] P.R. Shepherd., P.S.A. Evans., B. J. Ramsey & D. J. Harrison. “Assessment of Conductive Litho graphic Films for Microwave Applications”. 25th Automated R.F. and Microwave Measurement Society Conference, Limpley Stoke, Bath, UK, 31st October - 1st November 1996.

[3] P. S. A. Evans, B. J. Ramsey, D. J. Harrison & P. R. Shepherd. “Further Developments of Microwave CLFs”, 26th Automated R.F. and Microwave Measurement Society Conference, Abbey Hotel, Malvern, 7-8th April 1997.

[4] P. R. Shepherd, P. S. A. Evans, B. J. Ramsey & D. J. Harrison. “Lithographic Technology for Microwave Integrated Circuits”, Electronics Letters Vol. 33, No. 6, pp. 483-4, 13th March 1997.

Via type	L (pH)	R (Ω)	C (fF)
Ink	370	0.018	160
Paint	380	0.340	280
Epoxy	488	0.426	6.2

Table 1: Via Equivalent Circuit Values

Capacitor Area (mm^2)	C_C pF	L_C pH	$C_{E1,2}$ pF
1	1.92	650	0.29
4	8.14	827	0.42
16	26.0	421	1.18
25	45.0	337	1.56

Table 2: Laminated Capacitor Equivalent Circuit Values

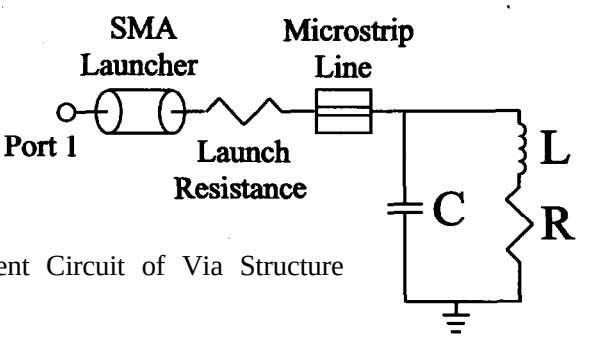

Figure la: Equivalent Circuit of Via Structure

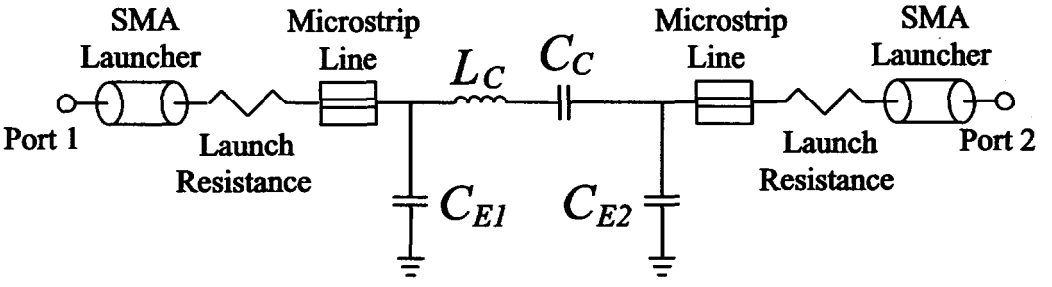

Figure lb: Equivalent Circuit of CLF Capacitor