Characterization of CMOS Spiral Inductors

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Abstract

In this work "full-wave" simulations of integrated inductors are presented and compared with measurements of fabricated CMOS chips. The good agreement between measurements and simulations demonstrates the accuracy of the tool, which is, hence, a cheaper alternative to experimental characterization. Furthermore, the proposed approach may give precious hints for performance improvements, by making internal device fields and currents available for the VLSI designer and providing compact, most effective, equivalent models.

I. Introduction

CMOS technology is actually the only option able to fit the low-cost constraints and to integrate digital and analog functional modules on a single chip. This capability is required by many consumer-electronics products, such as cellular or cordless phones, pagers, WLAN interfaces, etc.

The reliability and efficiency of CMOS-RF blocks can be improved by realizing on-chip passive devices, expecially high-Q inductors [l]. These are customarily obtained by patterning a spiral shape on a metal plane: in principle, building small-size, planar inductors is difficult because of the inherently non-planar behaviour of the coil (the magnetic flux being orthogonal to the current-flow plane), and of the lack of magnetic materials in a standard CMOS technology. Moreover, CMOS-compatible inductors deviate from the ideal behaviour, due to several additional causes: the non-negligible resistivity of metal lines causes the inductor to have a high series resistance limiting its performance at low frequencies, while the capacitive coupling to the lossy silicon substrate is responsible for the degradation of the Q factor at higher frequencies [2].

A sensible characterization of this behaviour, although being rather a difficult task, is hence of crucial importance. Straightforward geometrical reasoning can be exploited to describe the inductor at a sufficient degree of accuracy only for extremely simple cases [3]. As soon as parasitic components become significant, more sophisticated techniques need to be used. A comprehensive approach, suitable for this task, consists of the distributed solution of the electromagnetic propagation problem. Numerical techniques can be applied, by solving the Maxwell's equations over a given domain: by means of proper discretization algorithms, a high degree of accuracy on geometrical and physical details can be attained.

Even if, because of their inherent computational demand, "full-wave" analysis techniques can hardly be applied at the whole-chip level, they can be exploited, within a hierarchical design flow, to extract an accurate and physically-grounded characterization of compact, synthetic models of critical propagation regions. Nevertheless, the purpose of distributed modeling is much wider than this: a richer set of information can be obtained, including, e.g., spatial distribution of field and current densities. Such a knowledge, in turn, may help designers to gain physical understanding of the device behaviour.

In this work, a 3D, "full-wave", time-domain EM simulator, developed at the University of Perugia and based on the FDTD algorithm [4], has been applied to the characterization of spiral integrated inductors. A number of chip prototypes, integrating more than twenty spiral inductors of different shapes has been fabricated and measured. The good agreement with simulation results witnesses the accuracy of the "full-wave" approach, and demonstrates that it can be safely exploited, in spite of much more time- and cost-expensive experiments, for equivalent circuit characterization.

Then, to demonstrate the insight power of the method, the actual behaviour of currents and fields has been extracted and discussed.

II. Method and measurements

The adopted simulation scheme allows for the "full-wave" solution of Maxwell's equations, which is carried out by means of a "Finite-Difference Time-Domain" (FDTD) discretization algorithm: implementation and main characteristics of the code have been discussed elsewhere [5].

The analysis proceeds as follows: first, a gaussian pulse is injected into the inductor network, by using a "lumped" voltage generator and a series resistance [6]. Then, "full-wave" propagation of the pulse, which inherently accounts for parasitic paths of any kind, is simulated by the FDTD algorithm, providing the time-domain inductor response; a DFT transform is eventually applied to extract impedance spectral components. Post-processing options include Q-factor computation and the extraction of frequency-domain field and current surfaces on arbitrary cross-sections.

A schematic view of an example of fabricated device is shown in fig. 1. A standard CMOS fabrication process *(Alcatel CMOS 0.35 mm)* is assumed: fig. 2-(a) shows a SEM micrograph of the DUT. The considered inductor

is obtained by a square spiral pattern, featuring two turns on the M5-layer and a return path on the M4-layer. The width of the spiral legs is W = 9 mm, and the spacing is S = 4 mm (see fig. 1). The metal wires are insulated from the silicon layers by a SiO_2 layer; below, an epi-layer and a thick, rather conductive, silicon substrate axe placed. The device is designed for GSG probe measurements with a 150 mm pitch and the pad dimensions are 100 **x** 100 mm. The SOLT calibration procedure has been performed by means of a calibration substrate. Finally, a pad de-embedding procedure has been carried out, using an integrated open structure, as shown in fig. 2-(b).

III. Results and discussion

For the present simulation purposes, the semiconductor layers are modeled as linear media, and characterized by a doping-dependent electrical conductivity, whereas silicon dioxide layers are assumed to behave as ideal dielectric materials. To obtain reliable results, particular attention has been paid at the discretization of the three-dimensional structure. Once the "full-wave" simulation has been carried out, a straightforward procedure [5] can be adopted to extract an equivalent circuit of the structure suitable for commercial CAD packages.

A comparison between simulations and experiments (for the spiral inductor considered above) is reported in fig. 3 and fig. 4. The good agreement demonstrates that the simulator can be safely exploited for the inductor characterization, being less time- and cost-expensive than experiments.

From fig. 3, the negative impact of parasitic phenomena can be appreciated, which reflects on rather poor values of Q (if compared with technologies more explicitly oriented to high-frequency applications). Nevertheless, as stated above, a strong need for the adoption of large-volume fabrication technologies exists, and the physical causes of the Q-factor degradation are worth to be investigated, both from a quantitative and a qualitative point of view.

The real and the imaginary parts of the impedance can be correlated to the equivalent resistance and inductance of the spiral, which are reported in fig. 4. At low frequency, the impedance is dominated by metal losses, and can be quite reasonably assessed by simple geometrical considerations; both experimental and simulation results are in agreement with such expectations.

As the frequency grows, substrate effects tend to gain importance, and become substantial near the self-resonance region, where the inductor behaviour suddenly turns into a capacitive one. At high frequencies, the current, in fact, is no longer confined into the metal pattern: displacement current becomes more and more significant, as shown in fig. 5. Here, the displacement current component $\frac{\partial D_z}{\partial t}$ computed at 10 GHz, is shown, being particularly evident in the inter-turn gap and thus witnessing the progressive coupling among adjacent legs (clearly, a similar behaviour is exhibited by the coplanar $\frac{\partial D_x}{\partial t}$ component, not shown). This eventually results in a short circuit among nested turns, which gives reason of the abrupt decrease of the inductance and allows for interpreting the high-frequency tail of the equivalent-resistance curve shown before (fig. 4): the coil, at increasing frequencies, tends to behave as a conductive plate, capacitively coupled with the substrate. A significant displacement current flows across the oxide layer: a strong current penetrates deeply into the substrate, thus resulting in a large energy loss, which is responsible for a Q-factor degradation at high frequencies [5].

A further loss mechanism is due to the penetration of the magnetic flux concatenated with the coil into the silicon, which induces parasitic currents to circulate below the coil itself. Fig. 6 makes such a statement evident: it refers to the y-component (which lays parallel to the silicon/oxide interface) of the conduction current, and clearly mark the "eddy" current path.

IV. Conclusions

In this work, a "full-wave", FDTD-based simulator, customized for the analysis and characterization of CMOS spiral inductors, has been presented. A number of spiral inductors has been fabricated on CMOS chips, and measurements have been carried out. The good agreement obtained between measurements and simulations demonstrates that the developed procedure is a useful, cheaper than experiments, aid for the extraction of compact device models, suitable for commercial CAD packages. Furthermore, powerful investigation capability of the electromagnetic numerical modeling have been exploited to illustrate the quite intricate substrate loss physics: we think that the availability of internal device fields and currents may give the designer useful hints for further improvements.

References

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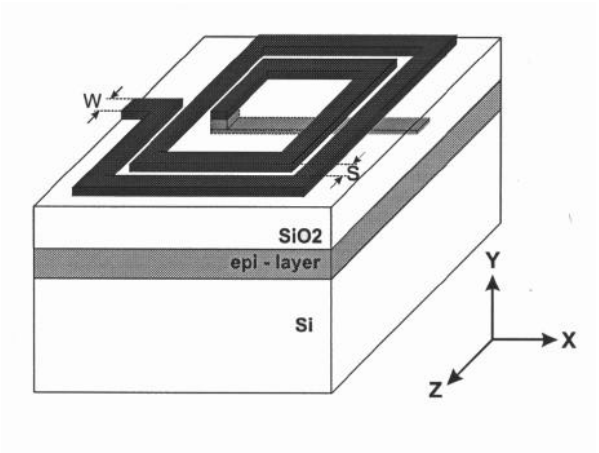

Fig. 1. Sketch of simulated spiral inductor.

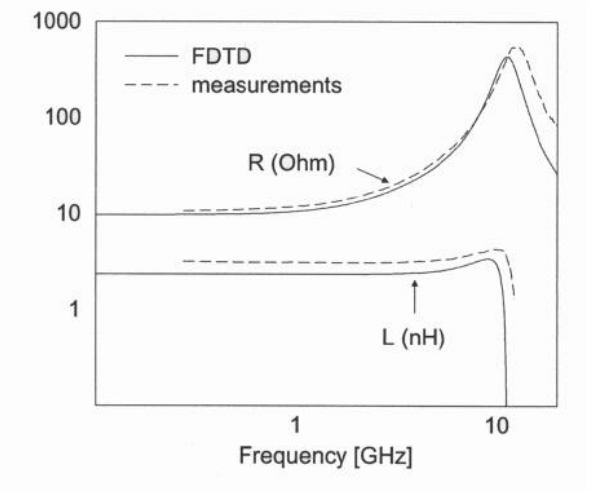

Fig. 4. Simulated and measured real and imaginary part of the impedance of the spiral inductor in fig. 1.

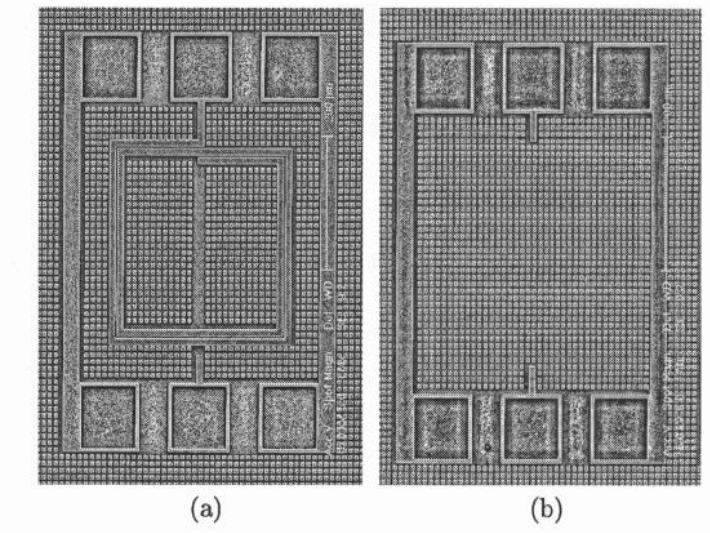

Fig. 2. SEM micrograph of the simulated inductor (a) and of the test structure for PAD de-embedding (b).

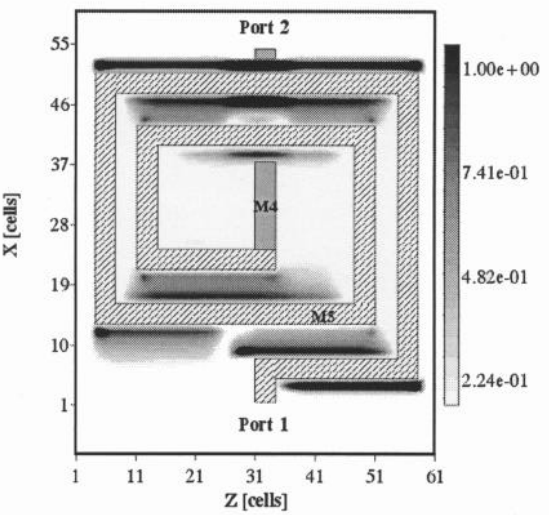

Fig. 5. Normalized modulus of x-component displacement current within the oxide @ 10 GHz in a planar section of the inductor.

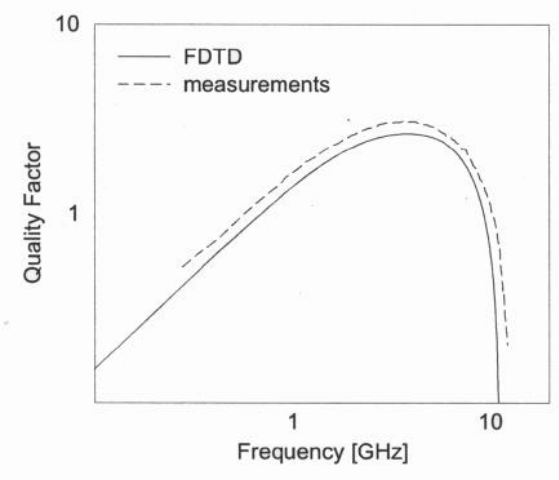

Fig. 3. Simulated and measured Q-factor for the CMOS spiral inductor of fig. 1.

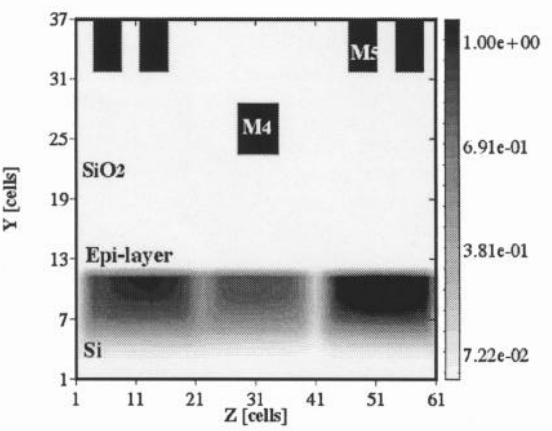

Fig. 6. Cross-sectional view of the normalized modulus of x-component conduction current @ 10 GHz.