

mm-wave Performance of 50nm T-Gate AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistors with f_T of 200 GHz

Xin Cao, Euan Boyd, Helen Mclelland, Stephen Thoms, Martin Holland, Colin Stanley, Iain Thayne

Nanoelectronics Research Centre, University of Glasgow, Glasgow G12 8LT, Scotland UK. Tel +44(0)141 330 6678

Abstract — By combining high resolution electron beam lithography, novel T-gate resist stacks, aggressively scaled vertical architectures and highly uniform, reproducible non-selective single “digital” gate recess etching techniques, we show it is possible to realise 50 nm gate length GaAs pHEMTs with f_T of 200 GHz suitable for applications beyond 100 GHz. This shows that by properly optimising and controlling critical parameters in an aggressively scaled GaAs pHEMT technology, excellent mm-wave performance can be achieved without the need to move to metamorphic GaAs or InP HEMT solutions.

I. INTRODUCTION

High performance devices that operate in the millimeter wave (30 to 300 GHz) frequency ranges will be major elements of future communication systems. InP based InAlAs/InGaAs high electron mobility transistors (HEMTs) are highly regarded for these application areas as they offer intrinsic speed and noise performance advantages over GaAs pseudomorphic HEMT (pHEMT) devices for a given gate length. Compared to InP HEMTs, GaAs pHEMTs benefit from a more mature fabrication process, larger wafer sizes and reduced substrate costs for a given wafer diameter and thus greater economies of scale, and higher reliability. Clearly however, for GaAs pHEMTs to be competitive with InP-based devices, the baseline performance should be at least comparable. Due to the lower mobility and sheet electron density of GaAs pHEMTs materials, they must have shorter gate length to achieve the same cut-off frequency as InP HEMTs.

One of the main challenges to realize short gate length devices is electron-beam lithography technology for T-gate fabrication. Conventional electron-beam lithography T-gate fabrication is commonly based on PMMA and related co-polymers[1,2]. In such resist stacks there is a relatively limited difference in the electron beam sensitivity of the resists and this limits the ultimate cross-sectional dimensions of the T-gates [3]. By contrast, UVIII is a Shipley DUV photoresist, which is almost five times more sensitive to electron beam exposure than PMMA thus enabling ultra-short footprint T-gates with larger cross sectional areas to be written at higher speeds [4]. The increased cross-sectional area of the gate results in reduced DC and RF resistance/inductance of the gate electrodes giving the highest performance mm-wave devices.

In this paper we report on the first published results of 50 nm T-gate devices made using bilayers of UVIII and PMMA resists and show that well scaled, optimised and highly engineered, reproducible, uniform 50 nm gate length GaAs pHEMTs have performance metrics that suggest they are well suited to applications beyond 100 GHz.

II. MATERIAL STRUCTURE AND DEVICE FABRICATION

The layer structure of the devices used in this work were grown in-house by molecular beam epitaxy (MBE) on a 3 inch diameter (100) GaAs substrate. The room-temperature epi-layer properties were measured using Van der Pauw structures giving sheet density of 4.4×10^{12} cm^{-2} and mobility of $4600 \text{ cm}^2/\text{Vs}$. After processing and wet etch removal of the GaAs cap room temperature sheet density of 1.5×10^{12} cm^{-2} and mobility of $5400 \text{ cm}^2/\text{Vs}$ were measured.

The 50nm HEMTs devices were realized using the in-house MMIC fabrication process. Ni-Ge-Au based ohmic contacts were annealed at 360°C using rapid thermal annealing, resulting in transistors with repeatable ohmic

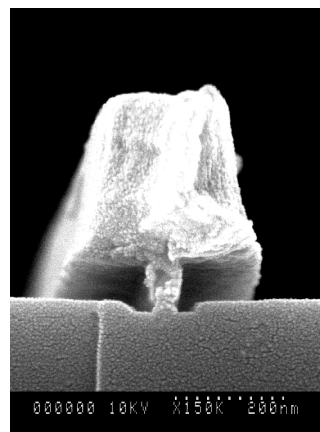
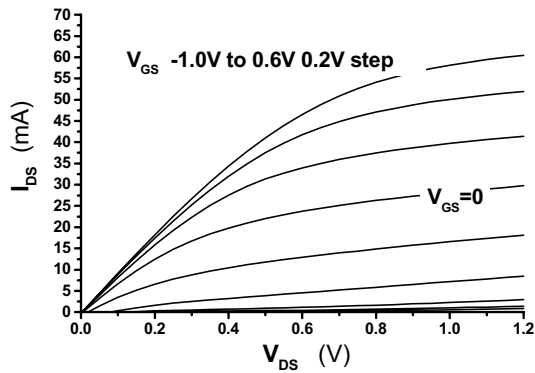
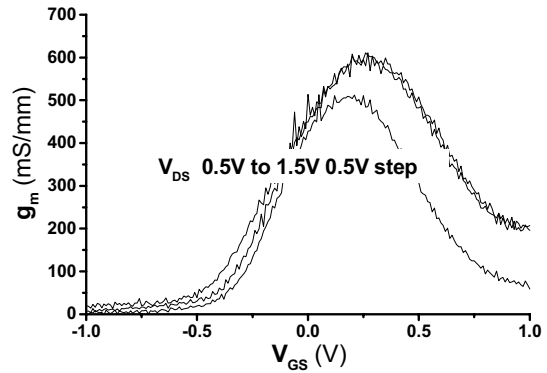


Figure 1 SEM image of the cross section of a fabricated T-gate from a real device.



(a) I-V characteristics



(b) g_m characteristics

Figure 2 Extrinsic DC output characteristics of $2 \times 50 \mu\text{m}$ 50 nm GaAs pHEMT

contact resistances around $0.1 \Omega\text{-mm}$. Wet-etch mesa isolation was performed using a 1:1:200 ammonia: hydrogen peroxide : water solution. The 50 nm T-gates were realized by electron beam lithography (Leica Microsystems Lithography LTD EBPg-5HR 100) utilizing a UVIII/PMMA resist stack [4]. Gate recess etching was performed using non-selective wet digital gate recess etch process[5]. Schottky gate metallisation was Ti-Pd-Au. Bond pad metallisation of 400nm Au was used to facilitate electrical connection to the devices. A selection of two finger devices with widths in the range $25\text{-}75 \mu\text{m}$ were fabricated in coplanar waveguide technology, to facilitate direct on-wafer mm-wave characterization.

Figure 1 shows scanning electron microscope (SEM) image of the cross section of a fabricated T-gate taken from a real device. It clearly shows that a gate recess width of 30nm each side of the gate was achieved.

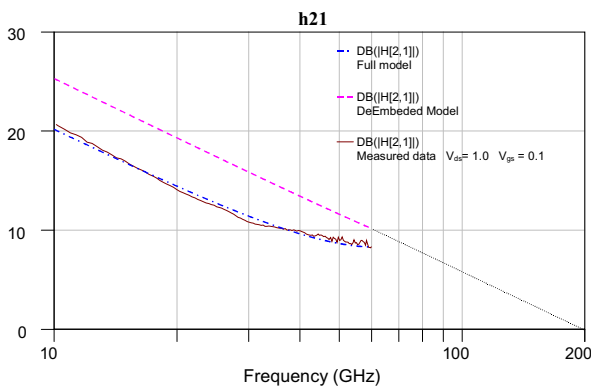


Figure 3 Measured and modeled $|h_{21}|$ against frequency

III. DEVICE PERFORMANCE

Figure 2 shows the measured extrinsic DC output characteristics of a $2 \times 50 \mu\text{m}$ 50 nm T-gate device. The device has a measured peak extrinsic DC g_m of 610 mS/mm and a threshold voltage (V_{th}) of -1.2V .

On-wafer S-parameter measurements were performed from 0.04-60 GHz over the full bias range, using an Anritsu 360B Vector Network Analyser fitted with on-wafer Picoprobes from GGB. Calibration was performed using Cascade Microtech's Impedance Standard Substrate (ISS) and the LRRM technique. FET model extraction was performed at each bias point to study the performance. Figure 3 shows a plot of measured and modeled $|h_{21}|$ against frequency for a $2 \times 50 \mu\text{m}$ gate width device biased at $V_{ds}=1.2\text{V}$, $V_{gs}=0\text{V}$. At this bias, using -20dB/decade rolloff, the device has an extrapolated peak f_T of 200 GHz – to our knowledge, the highest performance GaAs pHEMT reported.

The mechanical gate yield on 12mm by 12mm samples containing 112 devices, which mainly depends on gate lithography and gate recess etching, was 99%. The DC and microwave performance yield were 95% for $2 \times 25 \mu\text{m}$ gate width devices and 90% for $2 \times 50 \mu\text{m}$ devices.

IV. CONCLUSION

In conclusion, we report the fabrication of aggressively scaled 50nm T-gate GaAs pHEMTs realised using a UVIII/PMMA bilayer and a non-selective “digital” wet chemical gate recess etch which resulted in highly uniform, reproducible device characteristics. Initial measurement results show very promising mm-wave performance with an f_T of 200 GHz obtained from a $2 \times 50\mu\text{m}$ gate width device biased at $V_{ds}=1.2\text{V}$ – to our

knowledge the highest performance GaAs pHEMTs device layer structure and fabrication procedures to improve both the DC and RF performance of these devices, these initial results show that well engineered, controlled technology offers the possibilities for the realisation of GaAs pHEMT MMICs for applications beyond 100 GHz.

REFERENCES

- [1] Y.Yamashita, A.Endoh, K.Shinohara, M.Higashiwaki, K.Hikosaka, T.Mimra, S.Hiyamizu, T.Matsui, "Ultra-Short 25-nm-Gate Lattice-Matched InAlAs/InGaAs HEMTs within the Range of 400 GHz Cutoff Frequency", IEEE Electron Device Letters, Vol.22, 2001, pp367-369
- [2] T.Enoki, M.Tomizawa, Y.Umeda, and Y.Ishii, "0.05um Gate InAlAs/InGaAs High Electron Mobility Transistor and

reported. Whilst work is ongoing to further optimize reduction of Its Short Channel Effects", Jpn.J.Appl.Phys. Vol33, 1994 ,pp798-803

- [3] Y.Chen, T.Lodhi, H.McLelland, D.L. Edgar, D.Macintyre, S. Thoms, C.R. Stanley, I.G. Thayne, "First demonstration of InGaAs/InAlAs HEMTs using T-gates fabricated by a bilayer of UVIII and PMMA resists", 8th IEEE International Symposium on High Performance Electron Devices for Microwave and Optoelectronic Applications, 2000, pp. 202-205
- [4] Y.Chen, D.Macintyre, and S.Thoms, "Electron beam lithography process for T-and G-shaped gate fabrication using chemically amplified DUV resists and PMMA", J. Vac. Sci. Technology, B17, 1999, pp. 2507-2511
- [5] Xin Cao, Iain Thayne, "Novel high uniformity highly reproducible non selective wet digital gate recess etch process for InP HEMTs", Microelectronic Engineering, 2003, Accept for publication.