

Perspective of RF CMOS/Mixed Signal Integration in Next Generation Satellite Systems

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Modern satellite systems require integrated circuits capable of meeting performance, power consumption, price, radiation and integration requirements. As satellite systems evolve to large digital payloads with phased array antennae, highly integrated mixed signal and RF ICs are becoming critical to overall system performance. Integration is also critical to reducing size, mass and cost. Ultra-Thin-Silicon, or UTSi, CMOS is a modern, high yield silicon on sapphire technology which provides natural radiation hardness with high volume commercial CMOS manufacturing. We discuss previously unavailable levels of RF mixed signal and optical integration and potential future applications.

Introduction

Satellite industry deeply evolved in the last years to support emerging broadband services. Satellite prime contractors and space hardware manufacturers must evolve as well put in place all the efforts to keep their competitiveness. Technology integration, cost reduction and system miniaturisation are business drivers and key factors to be considered in defining R&D strategies.

In this scenario technology partnerships become a key strategy reducing the gap between state of art semiconductor and device processes and their reliable use for space systems. In this paper we describe one of the newest variations on the CMOS theme: commercial quality CMOS built in silicon on sapphire called UTSi CMOS. While the CMOS circuitry is both high speed and low power, it is sapphire's properties which create new opportunities. As a virtually perfect insulator, sapphire allows RF and mixed signal integration including high-Q passive devices. And sapphire's transparency from UV through IR enables new optical integration. The impact of these capabilities on satellite systems is presented.

UTSi Technology description

Ultra Thin Silicon, UTSi, CMOS is a fully depleted CMOS technology made in a 100 nm thick Si film on sapphire. Advantages of forming UTSi CMOS transistors on a pure sapphire substrate are manifold including the following:

- ⌘ Inherent radiation hardness
- ⌘ Low capacitance, hence high speed at low power
- ⌘ Fully depleted operation, improving linearity, speed, and low voltage performance
- ⌘ Excellent RF performance:
 - ⌘ f_{max} typically 3X f_t (60 GHz at $L = 0.5 \mu m$; and 100 GHz at $0.25 \mu m$)
 - ⌘ very high linearity (+38 dBm IP3 mixers)

- ⌘ high Q integrated passives ($Q_L > 40$ at 2 GHz for 5 nH inductor)
- ⌘ high isolation (>50 dB between adjacent devices)
- ⌘ Integrated EEPROM available without additional masks or process steps
- ⌘ Multiple threshold options without additional cost
- ⌘ An extremely low-loss substrate at RF frequencies
- ⌘ Excellent ESD protection with low parasitics
- ⌘ New design options over GaAs due to availability of good PMOS transistors
- ⌘ Optically transparent substrate for use in optical applications
- ⌘ Processed in standard CMOS facilities on large wafers

Figure 1 shows a cross-sectional comparison between conventional CMOS and UTSi CMOS.

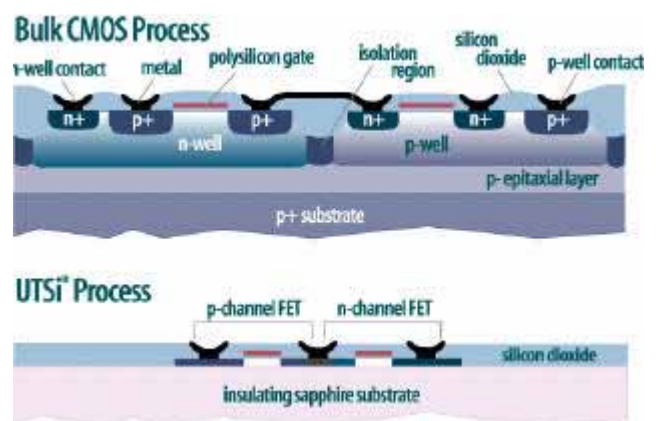


Figure 1. Cross-sectional view of bulk Si CMOS (top) and UTSi CMOS (bottom) showing reduced complexity and parasitics thanks to UTSi CMOS' sapphire substrate.

RF Performance

RF performance of mixers, PLLs, switches, passive devices, EEPROM and digital blocks has been discussed previously and will serve as a starting point for the current discussion.[1] A first example of the impact of integration is shown in Figure 2.

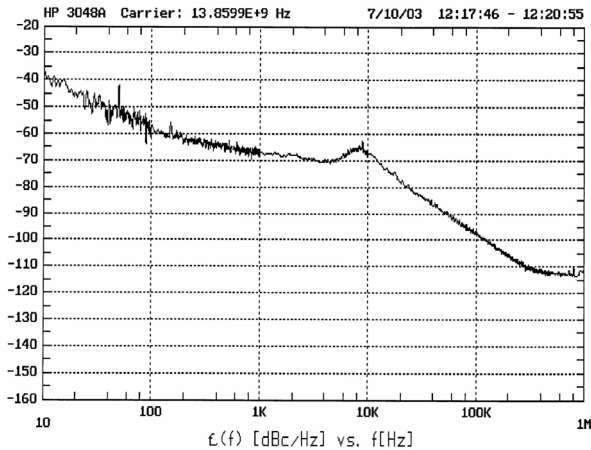


Figure 2. Alenia Spazio Ku Band (14 GHz) PLL based on Peregrine Fractional Synthesizer

Figure 2 shows a phase noise plot from a delta-sigma modulated PLL exhibiting -70 dBc/Hz phase noise at 13.8 GHz carrier, 10 kHz offset and -100dBc/Hz@100 kHz, and less than 300 Hz step size. Reference frequency is about 50 MHz. Since the chip is entirely CMOS, addition of 5,000 gates of digital logic converts a standard integer-N PLL into the DSM PLL. Flexibility was built into the chip, with both a Mash 1-1 and Mash 1-1-1 architecture as well as selectable charge pump or up-down outputs. Such built-in flexibility reduces inventory and development cost for many applications.

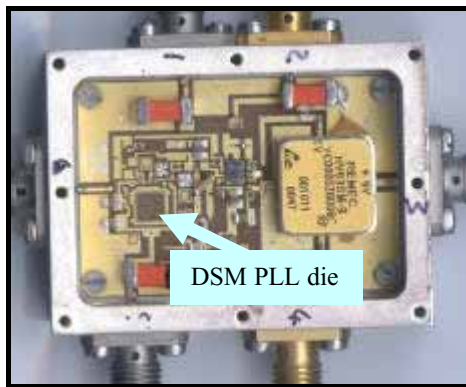


Figure 3. Photo of a 6 GHz synthesizer based on DSM PLL with phase noise of -92 dBc/Hz (step size of 114 Hz)

Area savings can be seen in Figure 3, which shows a complete Ku band synthesizer in 2.5 x 3.75 cm. As can be seen, the VCO is substantially larger than the DSM PLL die. Obviously, the next level of integration is to include the VCO.

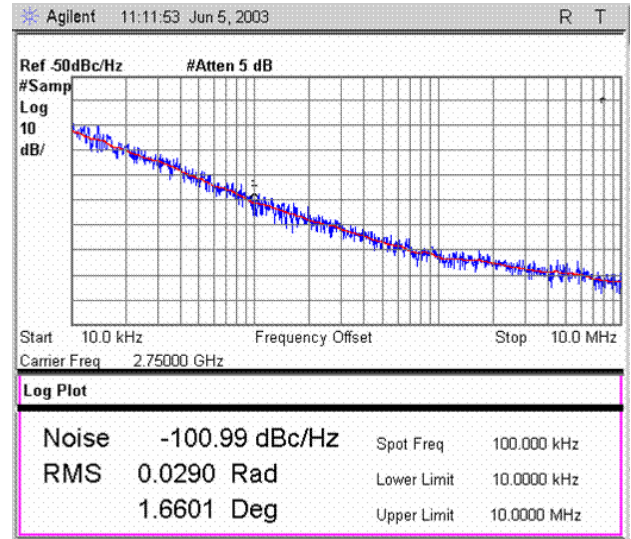


Figure 4. Phase noise plot of a fully integrated 2.75 GHz VCO showing better than -100 dBc/Hz @ 100 kHz offset.

Figure 4 shows a phase noise plot of a fully integrated VCO operating at 2.75 GHz. Close-in phase noise of -100 dBc/Hz at 100 kHz offset meets many system application requirements such as telemetry and command transponders. The VCO consumes about 2 mm² of chip area and can be integrated onto the DSM PLL shown in Figure 3 without any increase in die area, thereby substantially reducing the area of the synthesizer.

RF Integration Example

The key benefit of a sapphire substrate is very high levels of RF integration, specifically including a high percentage of passive devices. Figure 5 shows the block diagram of such integration: a single chip, dual band, high anti-jam GPS receiver front end.

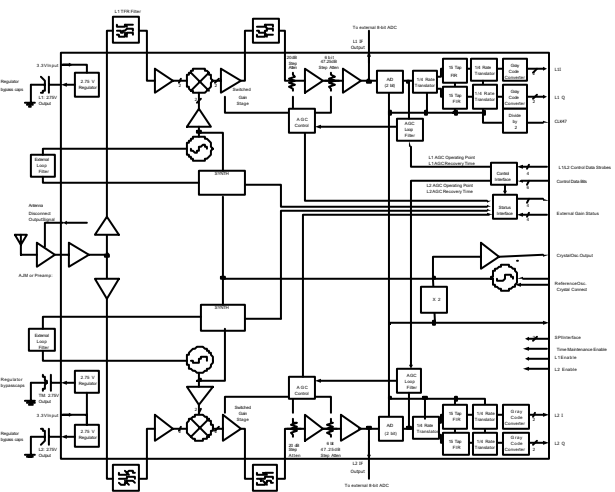


Figure 5. Block diagram of single chip, dual band, high A/J GPS receiver.

This chip includes virtually all active and passive components with the exception of the PLL loop filters elements (due to their large values); four SAW filters; and about a dozen decoupling capacitors. Channel isolation is provided by tuned RF amplifiers rather than a diplexer to save area. Each channel's gain control is an all digital loop based on two digital step attenuators: one at 1 bit and 20 dB and the other at 6 bits and 30 dB.

Since both channels must operate simultaneously, high isolation between the two synthesizer loops, especially on spurious noise, is required. To achieve this, one PLL is an integer-N device and the other a fractional-N device. This ensures that the spurious tones are never the same between the two channels. In addition, about 5k gates of digital signal processing is included to implement a quarter-rate conversion and digital filtering.

Combining these features into a single chip enabled substantial system-level advantages over the previous solution. Specifically, area reduction of more than 90%; power reduction of more than 60% and component number reduction of more than 90% were achieved.

Photonic Applications

Since sapphire is transparent from UV to far IR, UTSi CMOS has been applied to make high performance parallel optical interconnects. Figure 6 shows a module which is a 10 Gbps bi-directional (transmit and receive) parallel optical module made on UTSi CMOS. By flip-chipping VCSEL lasers and P-i-N photodetectors onto circuits designed to drive them (laser drivers and TIA/LA, respectively), virtually all bonding parasitics and alignment issues are resolved. Laser cutting of alignment holes in the sapphire substrate provides a mechanical self-alignment feature which ensures reliable optical coupling.

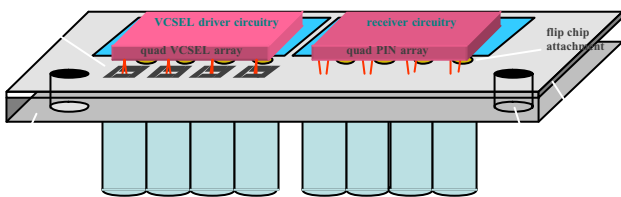


Figure 6. Flipped Optical Chips on UTSi, FOCUTS, consists of VCSEL arrays and photodetector arrays flip chip attached to their respective driver circuits.

Figure 7 shows a waterfall chart from a 2.5 Gbps optical link of Figure 6 with a bit error rate of 1×10^{-10} at input optical power of -13 dBm. Each channel consumes approximately 100 mW of power. The entire module is 0.5x1x2 cm and can be configured in any combination of TX and RX for each of the 12 channels. Two dimensional arrays such as 2x12 are also possible in the same basic configuration.

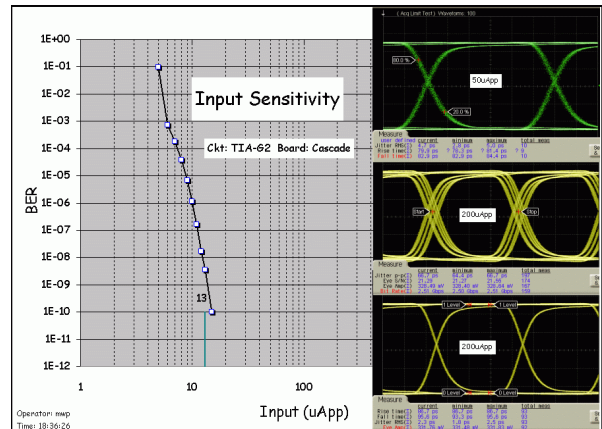


Figure 7. Waterfall chart and eye diagrams from an integrated optical link of Fig.6.

13 GHz (Ku band) operation

Because of its CMOS base, this technology scales in speed and power with gate length. Figure 8 shows an f_{max} comparison to conventional CMOS performance. The high f_{max} is due to low substrate losses and low parasitic capacitances within the transistor which enables frequency of operation at the product level up through Ku band. Fig. 9 shows simulated performance of a /4 prescaler operating at 13.5 GHz in 0.25 μ m channel length devices. Input sensitivity is -5 dBm; output power is 0 dBm and power dissipation is less than 35 mW.. Since the 0.5 μ m transistors support virtually all RF functions up through 6 GHz, it is not surprising that the 0.25 μ m technology can support operation up through Ku band, opening significant new integration opportunities.

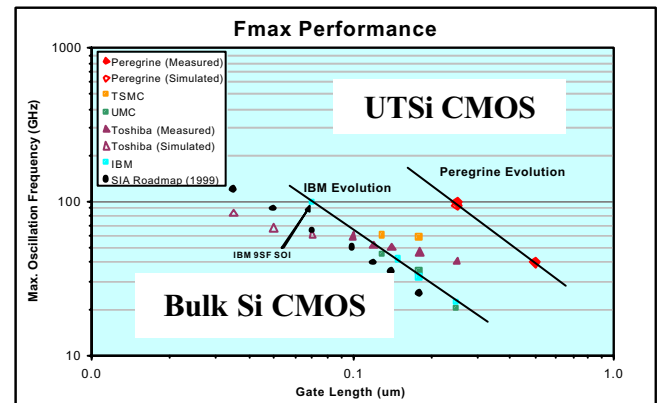


Figure 8. f_{max} comparison for bulk Si CMOS and UTSi CMOS, showing to achieve 100 GHz bulk S requires 0.07 μ m technology while UTSi CMOS requires only 0.25 μ m.

Use of CMOS devices like microwave prescalers up through Ku band offers a significant power requirement reduction, close to one order of magnitude, with respect to corresponding functions using Gallium Arsenide processes. This is a very significant result for space equipment architects in their effort to reduce dimension and power for next generation products.

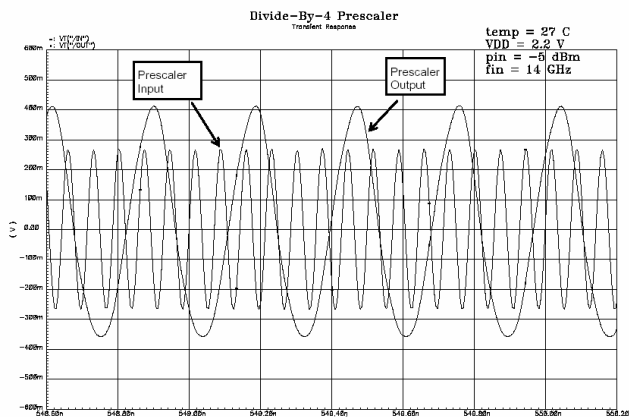


Figure 9. 14 GHz (Ku band) 1/4 prescaler simulation.

Fig. 10 shows the technology could apply to creating highly integrated T/R modules. In this concept, where size, weight, performance and power consumption are critical, a highly integrated RF ASIC can provide all but LNA and PA functions. The green highlighted functions can be delivered on a single IC, including I/O switches, digital step attenuators, digital phase shifters, RF amplifiers, voltage regulators and control CMOS.

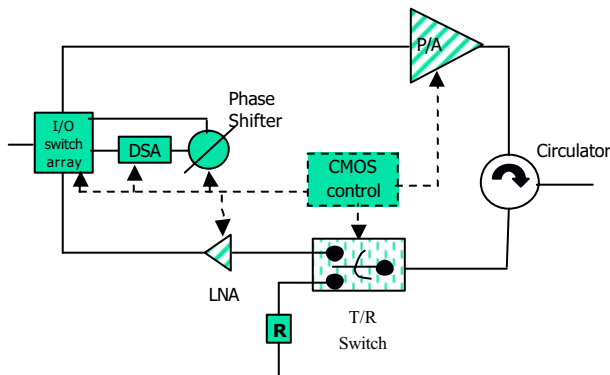


Figure 10. Transmit/receive, T/R, device with green blocks integrated into a single IC. In 0.25 μm technology, such devices can operate through Ku band (13 GHz).

Since a major portion of T/R module cost is assembly and test, the highly integrated solution has potential for substantial cost reduction. A primary savings is that test is performed at the wafer level where testing is very efficient and early in the manufacturing cycle. Since the core technology is CMOS, high yield is to be expected. Other savings occur in touch labor and parts count. We estimate savings potential up to 75% in parts count, 50% in area and 50% in cost.

Future potential

Additional functionality can be integrated to enable substantially new opportunities for space-based systems. For example, the functionality of T/R devices shown in Fig. 10 can be enhanced by addition of block down converters and A/D converters to provide digital output, enabling advanced functionality such as digital beam

nulling. For a 10 bit A/D at 150 MSPS, 1.5 Gbps of data will be generated per T/R module, creating a potential data transmission issue. For a 500 element antenna, 1.5 Tbps of data transmission is required in a small space and without creating crosstalk or EMI issues. A solution for this is depicted in Fig. 11: an A/D converter is integrated along with an optical transmitter as shown in Fig. 6. A single channel of optical interconnect can handle the bandwidth demands of a T/R module for less than 100 mW; and with digital data reduction (decimation), a single fiber channel could handle multiple T/R modules.

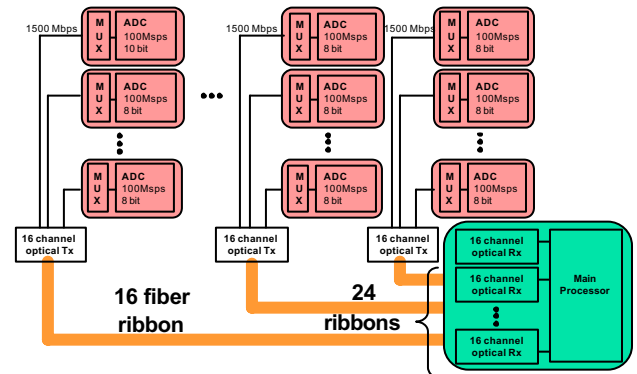


Figure 11. Phased array antenna with 384 elements delivering digitised data over fiber optic links. 24 16-fiber ribbons deliver >1 Tbps at 2.5 Gbps/channel.

A major cost of phased array antenna systems is assembly and wiring of the final system. Getting signals into and out of T/R modules requires complex wiring harnesses and careful simulations. High bandwidth signals, power, ground, and digital control signals must be carefully coordinated and tested. Electro-magnetic interference, EMI, is a substantial element of system design. The system of Figure 11 offers relief and savings on all these factors through high levels of integration (size, cost and power savings) and optical interconnects (assembly complexity, size, EMI and cost savings).

Conclusions

A high performance Si CMOS technology on sapphire has substantial potential to change advanced satellite systems (as well as military and commercial systems). Based on standard CMOS processing, the technology offers all the advantages of CMOS while offering the benefits of an insulating substrate (high f_{max} , isolation, low power, low cost).

Reference:

1. R. Reedy, "Application of UTSi[®] CMOS On Sapphire to RF and Mixed Signal Requirements in Advanced Space Systems," EuMW 2002.
2. M.C. Comparini et al., "Next generation Payload Equipment for Broadband Multimedia Satellite Communication", EuMW 2002